

PCB Number: 17522

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| 62 | M.2 card-SSD | |
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| PAGE | TITLE | |
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| 84 | GPU VRAM 4 (4/4) (R) | |
| 85 | GPU CORE | |
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| 87 | GPU Switch (1/2) (R) | |
| 88 | GPU Switch (2/2) (R) | |
| 89 | GPU others (R) | |
| 90 | NFC (R) | |
| 91 | TPM Asset ID | |
| 92 | PS2 (R) | |
| 93 | Express Card# (R) | |
| 94 | Smart Card# (R) | |
| 95 | Translator | |
| 96 | MCU# (R) | |
| 97 | Intel LAN# (R) | |
| 98 | LAN Switch# (R) | |
| 99 | XDP&ITP# (R) | |
| 100 | Label RTC BATT | |
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| 102 | Power sequence | |
| 103 | Power delivery chart | |
| 104 | SMBUS table | |
| 105 | Clock MAP | |
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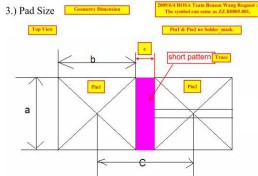
0805封裝尺寸/0402封裝尺寸/
0603封裝尺寸/1206封裝尺寸

封裝尺寸与功率關係：封裝尺寸与封裝的對應關係

| | |
|------------|------------------|
| 0201 1/20W | 0402=1.0mmx0.5mm |
| 0402 1/16W | 0603=1.6mmx0.8mm |
| 0603 1/10W | 0805=2.0mmx1.2mm |
| 0805 1/8W | 1206=3.2mmx1.6mm |
| 1206 1/4W | 1210=3.2mmx2.5mm |
| | 1812=4.5mmx3.2mm |
| | 2225=5.6mmx6.5mm |

Size Current

Short-PAD:
0402=ZZ.00PAD.M11=0.65A
0603=ZZ.00PAD.M21=0.875A
0805=ZZ.00PAD.M31=1.375A



| Dimension (mils) | a | b | c | d | e |
|------------------|----|----|----|---|---|
| Package | | | | | |
| 0402 | 26 | 11 | 35 | 5 | 5 |
| 0603 | 35 | 40 | 60 | 5 | 5 |
| 0805 | 55 | 45 | 76 | 5 | 5 |

TEST CONDITION FOR JUMPER (0W)

| Item | WR12 | WR08 | WR06 | WR04 |
|-----------------------|-----------|------|-------|-------|
| Power Rating At 70°C | 1/4W | 1/8W | 1/10W | 1/16W |
| Resistance | MAX.50mW | | | |
| Rated Current | 2A | 1.5A | 1A | 1A |
| Peak Current | 5A | 3.5A | 3A | 1.5A |
| Operating Temperature | -55~155°C | | | |

Design note:

| | | | | | |
|-----------|-----------|-----------|------------|-----------------------|-----------|
| 10KR3 | 10K | R | 3 | | |
| | value=10K | resistor | Size=0603 | | |
| SCD1U10V2 | S | C | D1U | 10V | 2 |
| | type=SMD | capacitor | value=0.1U | Withstang voltage=10V | Size=0402 |

BOM Configuration

| | |
|---|--|
| (R):Unmount | (X):For debug |
| (M):Mount for GPU M1-70 | (ZZ):Setup to Dummy |
| (HY2G):Mount for Hynix VRAM | (MS):Mount for Modern standby |
| (MC2G):Mount for Micron VRAM | (MUTE):Mount for MIC mute button |
| (SS2G):Mount for Samsung VRAM | (EYE):Mount for Eye comfort Button |
| (Nuvoton):Mount for Nuvoton TPM | (UMA):Mount for UMA |
| (Infineon):Mount for Infineon TPM | |
| (ST):Mount for ST TPM | |
| (TOUCH):Mount for ST TOUCH | |
| (UD):For USB Debug | |
| (PARADE):Mount for Parade re-driver | |
| (TI):Mount for TI re-driver | |
| (Nuvoton_/Infineon_):Mount for Nuvoton and Infineon TPM | (Nuvoton_/Infineon_/ST_):Mount for Nuvoton/Infineon and ST TPM |

Build Net==>
(Part Value):'{Value}''{Part Number}'
(PCB Footprint) :'{PCB Footprint}''{PCB Footprint}'
'{Value}''{Part Number}' '{PCB Footprint}''{PCB Footprint}'

Build BOM==>
#Reference\tPart Number\tSymbol\tGeometry\tF7\tFIN\tFIN1
{Reference}\t{Part Number}\t{Value}\t{PCB Footprint}\t{F7}\t{FIN}\t{FIN1}

#Reference\tPart Number\tSymbol\tGeometry\tF7\tFIN\tFIN1(Reference)\t{Part Number}\t{Value}\t{PCB Footprint}\t{F7}\t{FIN}\t{FIN1}

Build VRT==>
Item Number\tReference\t<Core Design>\tBOM1\tValue\tDescription
{Item}\t{Reference}\t{Part Number}\t{F7}\t{Value}\t{Description}

Build VRT==>
Item Number\tReference\t<Core Design>\tBOM1\tValue\tDescription {Item}\t{Reference}\t{Part Number}\t{F7}\t{Value}\t{Description}

Build OLB File==>
1. 先開啟廠商的DSN檔案，並且將要用的元件複製起來(如果是晶片組的話，只要其中一個即可)。
2. File->New->Design->將元件貼到Schematic的Page1，貼上之後會在Design Cache裡面出現一個*.OLB或者*.DSN檔案。
3. New->Library->將Design Cache裡面的*.OLB或者*檔案拖移到Library
4. 可以將Library裡面的*.OLB打開看其他的子元件(View->Package)
5. 將之儲存(Save)即可
6. 將*.OLB傳給Symbol team即可建此元件。

BD Information:

T=1.6 +/-0.1MM 6layers

L*W=245mmX 210mm

How to option FUSE

FUSE calculate Current:AI(A)

FUSE actual Current:A(A)

EXP calculate:

AI=X+0.8

1) A=AI+(+/-0.1)

2) AI+0.1<=A<=AI+0.4

Find==>Part Reference=(C|R)[2-9]

PCB BOARD SIZE
245mmX 210mm
6 Layer

Internal Slot/Header
Front/rear/side IO
Chipset/IC

NCP81220
(4 Phase 65W+2Phase)
P:46~49

DDR4 SO-DIMM
2400/2666 MHz
P:11 DIMM1

DDR4 SO-DIMM
2400/2666 MHz
P:13 DIMM2

Intel
Coffee lake-S LGA1151
S-LINE 6+2 65W
Quad code

AMD
R17M-M1-70
25W
64bit gDDR5
P:76~80

VRAM1 P:81
VRAM2 P:82
1G DDR5

PSU 19V
P:43

DP out P:57

21.5" LG panel P:55

EEPROM P:95

Translator IC P:95

Channel A 64 bit 1333/1600MHZ

Channel B 64 bit 1333/1600MHZ

DDP1

EDP

100MHz

2D WEBCAM\BT\Touch USB2.0 P:65

Card reader CONN P:33

USB2.0 *2 P:16 480Mb/S

USB3.1 x4 rear P:36,37

USB3.1 side with charger TI TPS2546 P:34

USB 3.1 Type C Side P:34

USB 3.1 *6 P:19 4.8Gb/S

PCB STACKUP 6Layer
245*210 mm
1.6mm

TOP
GND/PWR
L3-signal
L4-signal
GND
BOTTOM

PCB Color:==>
ET phase:Red
SDV phase:Blue
SIT/SVT phase:Green

Realtek ALC233VB3 P:27

MIC-IN side P:29
HP-OUT side

SATA *1 Slim ODD P:60

SATA *1 2.5" HDD P:60

SATA3.0 BUS

High Definition Audio

Speaker 2Wx2 P:29

Intel PCH
B360 PCH

SPI Flash ROM 16MB P:25

WLAN1 NGFF Card P:61

LAN RTL8111H P:97

RJ45 6KV P:32

SSD NGFF Card P:62

32.7K

100MHz
14MHz / 25MHz / 48MHz
48MHz
33MHz
14.318MHz

PECI

LPC BUS

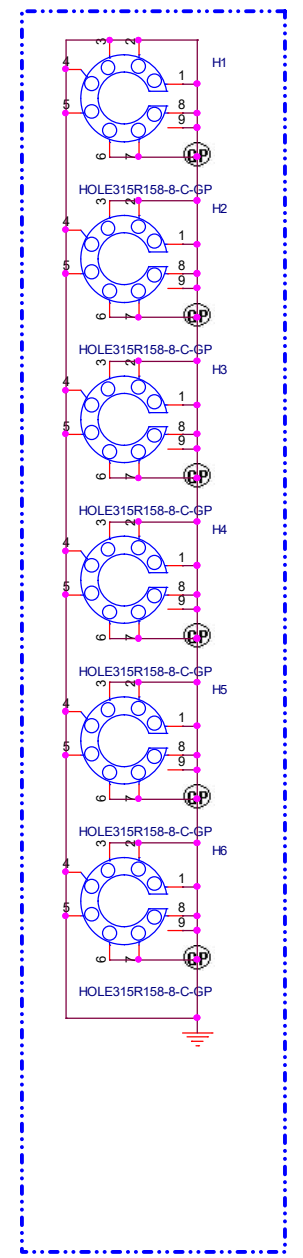
com port P:65

ECIO IT8378 P:24

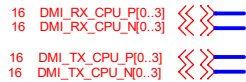
SPI Flash ROM 1MB P:24

SYS 1X4 FAN P:26

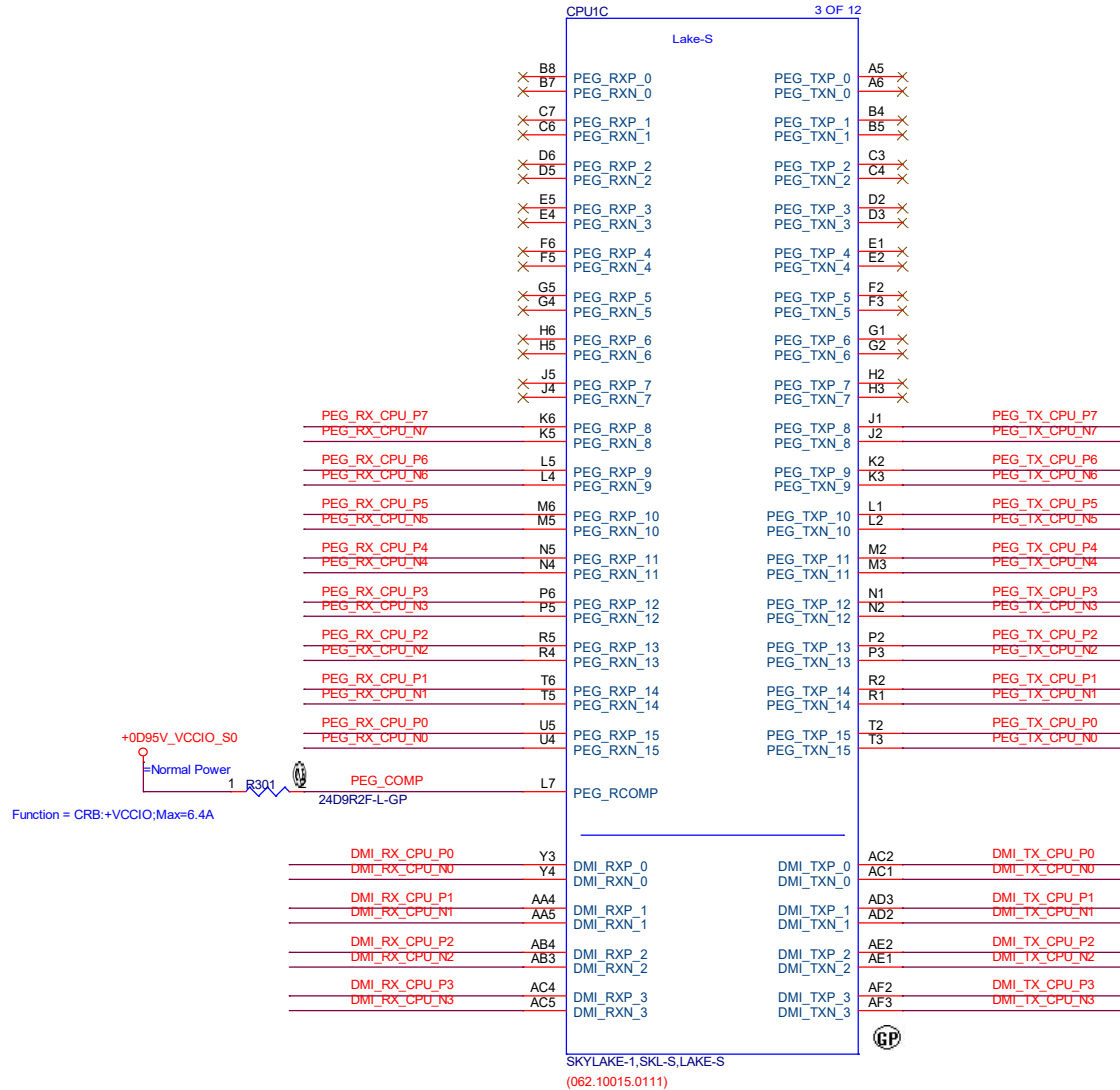
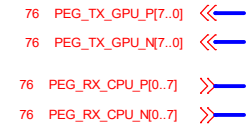
PCB MOUNTING HOLES-PTH



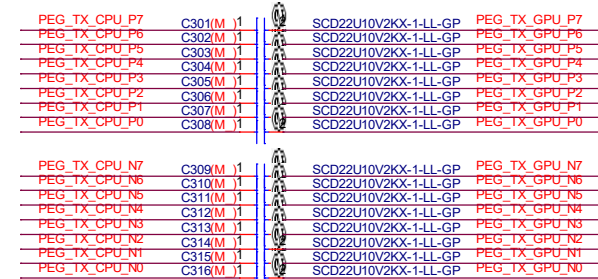
DMI



PCIEX8



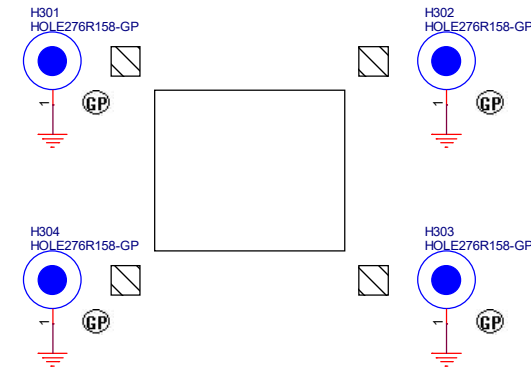
PEG Static Lane Reversal PCIe x8



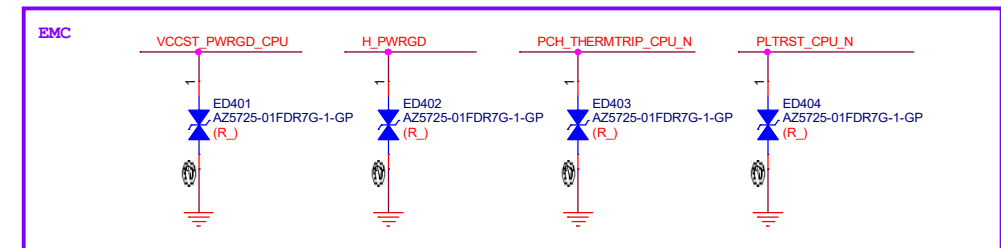
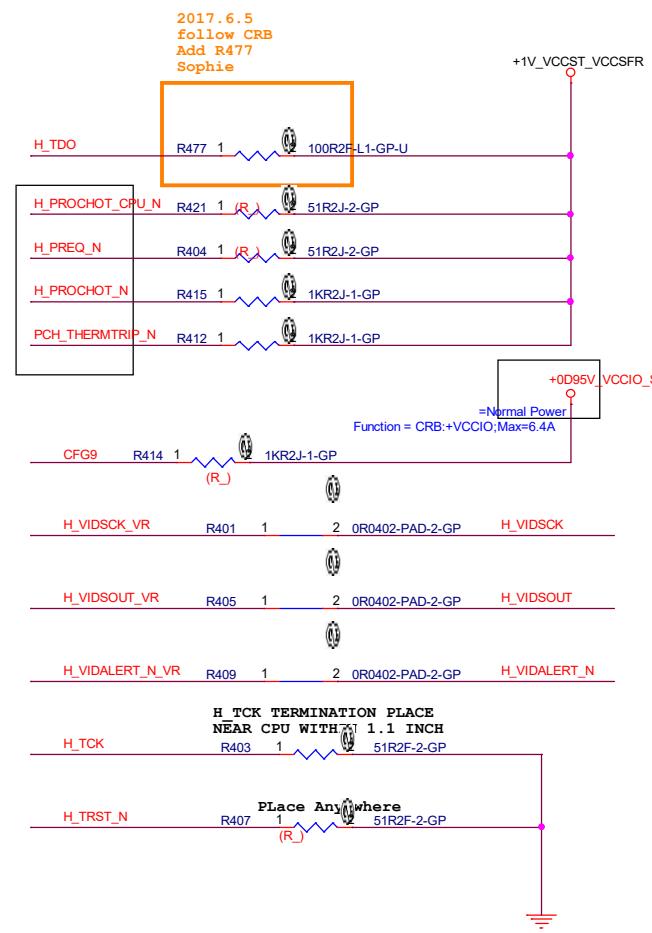
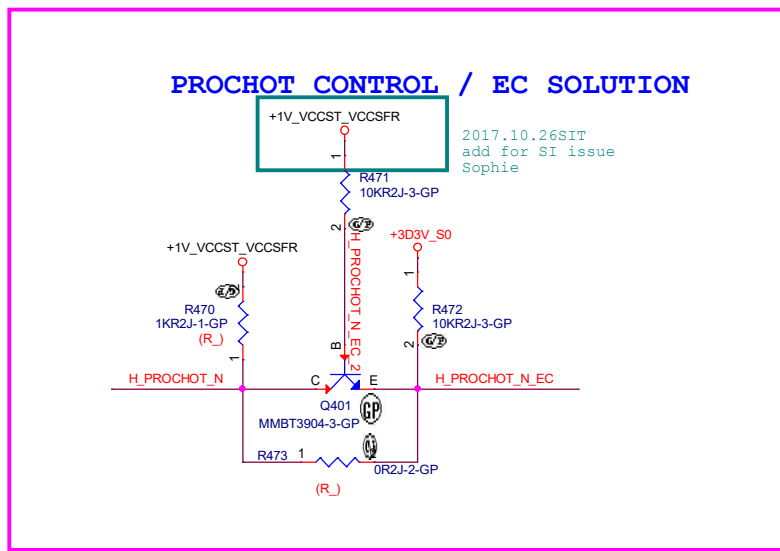
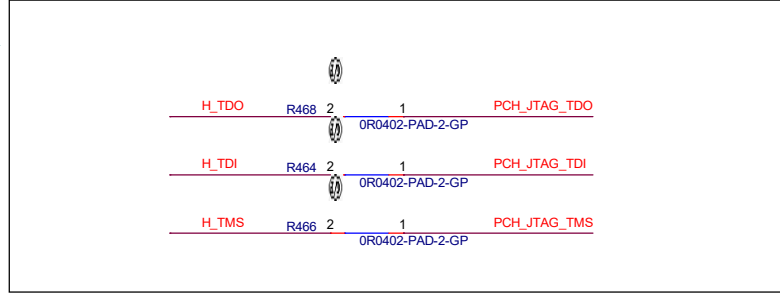
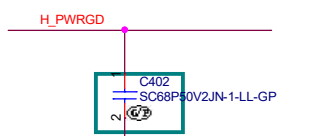
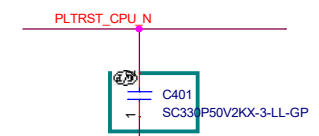
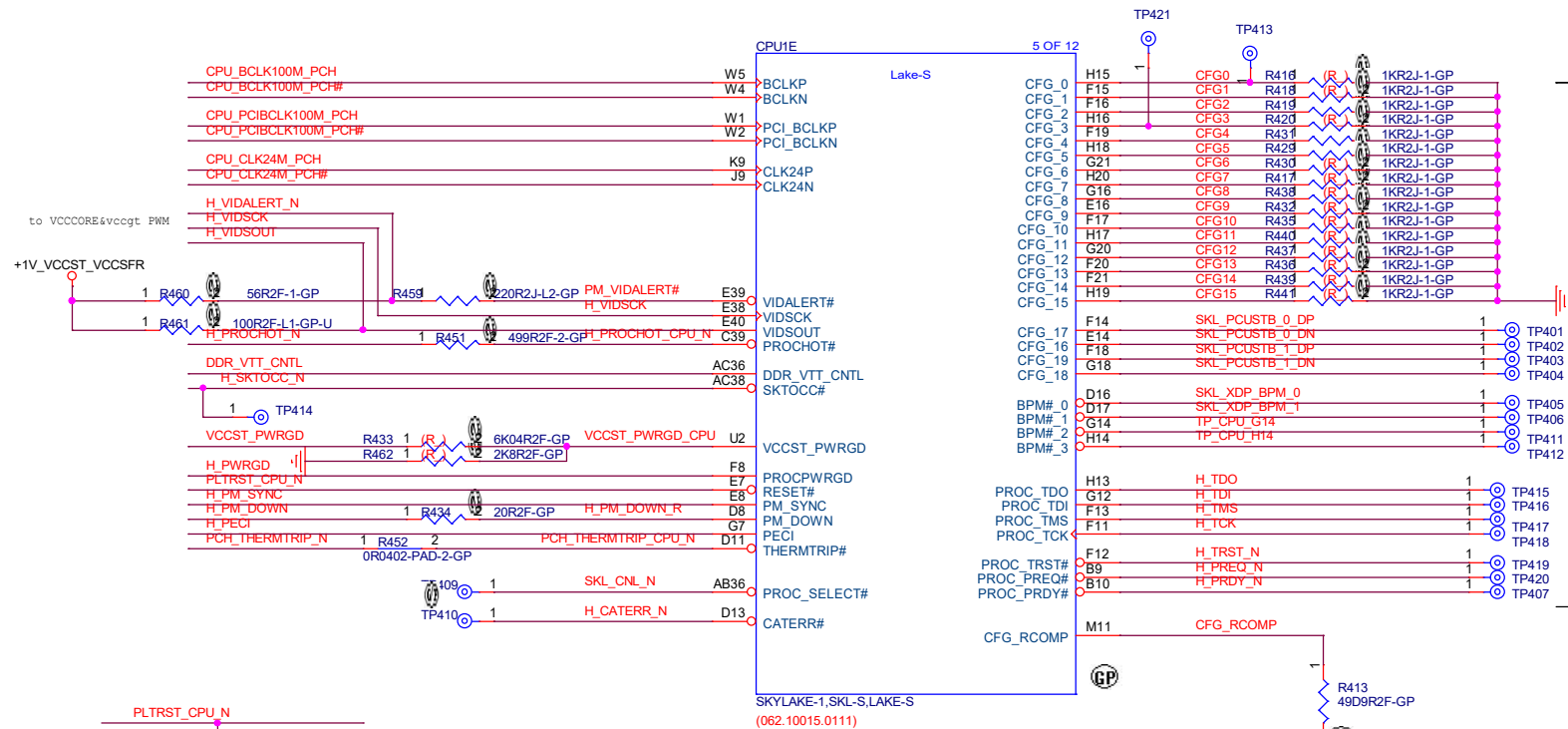
CPU MOUNTING HOLE-PTH

HOLE276R158

==>ZZ.00PAD.U61



46 H_VIDSOK_VR
46 H_VIDSOUT_VR
46 H_VIDALERT_N_VR
18 CPU_BCLK100M_PCH
18 CPU_BCLK100M_PCH#
18 CPU_PCBCLK100M_PCH
18 CPU_PCBCLK100M_PCH#
18 CPU_CLK24M_PCH
18 CPU_CLK24M_PCH#
46 H_PROCHOT_N
40 VCCST_PWRGD
20 H_PWRGD
17 H_PM_SYNC
17 PLTRST_CPU_N
17 H_PM_DOWN
17 PCH_THERMTRIP_N
17,24 H_SKTOCC_N
51 DDR_VTT_CNTL
17,24 H_PECI
40 VCCST_PWRGD_CPU
20 PCH_JTAG_TDO
20 PCH_JTAG_TDI
20 PCH_JTAG_TMS
20 H_TCK
21 H_TRST_N
21 H_FREQ_N
21 H_PRDY_N
24 H_PROCHOT_N_EC



| Signal Name | Description | Dir. | Buffer Type | Link Type | Availability |
|-------------|--|------|-------------|-----------|---|
| CFG[19:0] | <p>Configuration Signals: The CFG signals have a default value of '1' if not terminated on the board. Refer to the appropriate platform design guide for pull-down recommendations when a logic low is desired.</p> <p>Intel recommends placing test points on the board for CFG pins.</p> <ul style="list-style-type: none">CFG[0]: Stall reset sequence after PCU PLL lock until de-asserted:<ul style="list-style-type: none">1 = (Default) Normal Operation; No stall.0 = Stall.CFG[1]: Reserved configuration lane.CFG[2]: PCI Express* Static x16 Lane Numbering Reversal.<ul style="list-style-type: none">1 = Normal operation0 = Lane numbers reversed.CFG[3]: Reserved configuration lane.CFG[4]: eDP* enable:<ul style="list-style-type: none">1 = Disabled.0 = Enabled.CFG[6:5]: PCI Express* Bifurcation<ul style="list-style-type: none">00 = 1 x8, 2 x4 PCI Express*01 = reserved10 = 2 x8 PCI Express*11 = 1 x16 PCI Express*CFG[7]: PEG Training:<ul style="list-style-type: none">1 = (default) PEG Train immediately following RESET# de assertion.0 = PEG Wait for BIOS for training.CFG[19:8]: Reserved configuration lanes. | I | GTL | SE | All processor lines. CFG[2], CFG[6:5] and CFG[7] are relevant for H and S-processor line only and test point may be placed on the board for them. |

CHANNEL A DIMM0

11 M_A_DQ[63..0] << >>

11 M_A_A[13..0] << >>

11 M_A_DQS_DP[7..0] << >>

11 M_A_DQS_DN[7..0] << >>

11 M_A_BA[1..0] << >>

11 M_A_BG[1..0] << >>

11 M_A_CLK0 << >>

11 M_A_CLK#0 << >>

11 M_A_CLK1 << >>

11 M_A_CLK#1 << >>

11 M_A_CS#[1..0] << >>

11 M_A_ACT# << >>

11 M_A_ODT0 << >>

11 M_A_ODT1 << >>

11 M_A_CKE0 << >>

11 M_A_CKE1 << >>

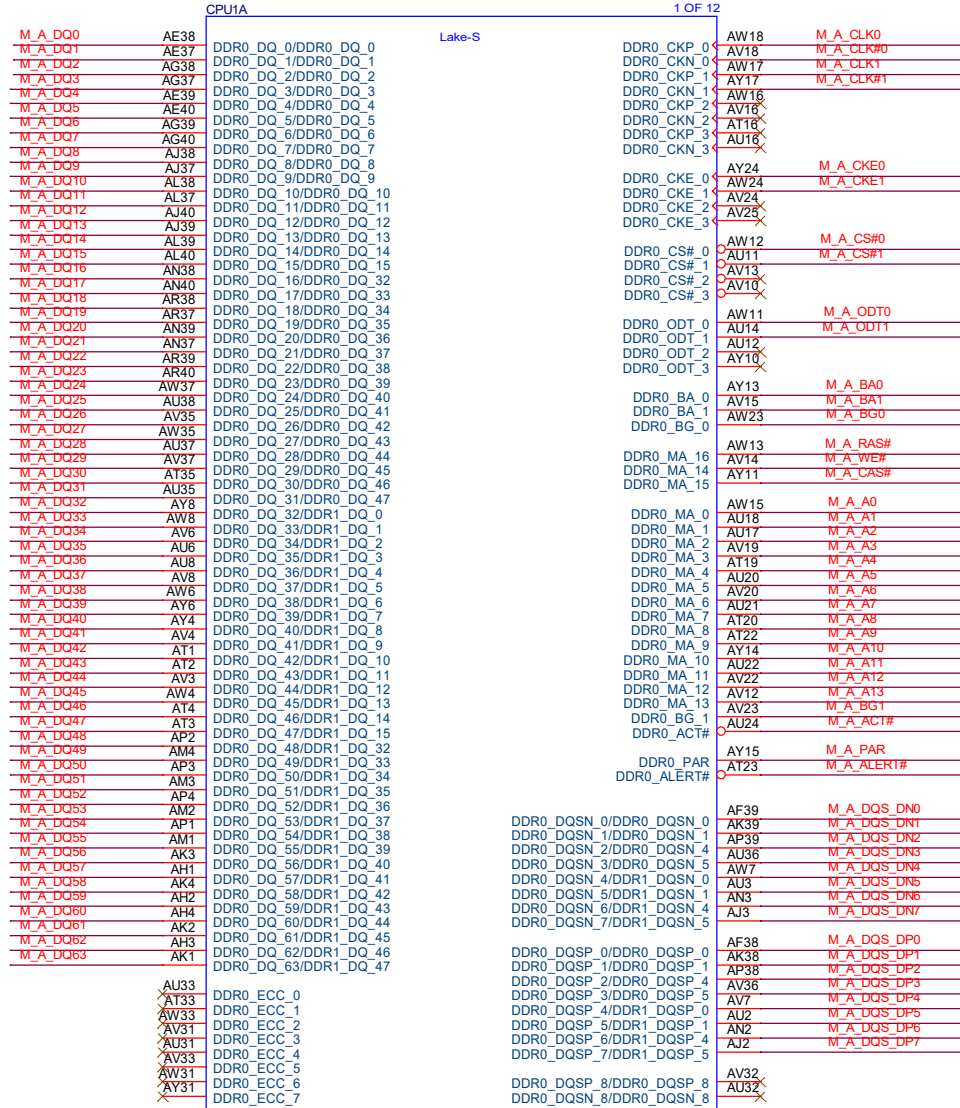
11 M_A_CAS# << >>

11 M_A_WE# << >>

11 M_A_RAS# << >>

11 M_A_ALERT# << >>

11 M_A_PAR << >>



CHANNEL B DIMM0

13 M_B_DQ[63..0]

M_B_DQ63
M_B_DQ62
M_B_DQ61
M_B_DQ60
M_B_DQ59
M_B_DQ58
M_B_DQ57
M_B_DQ56
M_B_DQ55
M_B_DQ54
M_B_DQ53
M_B_DQ52
M_B_DQ51
M_B_DQ50
M_B_DQ49
M_B_DQ48
M_B_DQ47
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M_B_DQ15
M_B_DQ14
M_B_DQ13
M_B_DQ12
M_B_DQ11
M_B_DQ10
M_B_DQ9
M_B_DQ8
M_B_DQ7
M_B_DQ6
M_B_DQ5
M_B_DQ4
M_B_DQ3
M_B_DQ2
M_B_DQ1
M_B_DQ0

13 M_B_A[13..0]

M_B_A13
M_B_A12
M_B_A11
M_B_A10
M_B_A9
M_B_A8
M_B_A7
M_B_A6
M_B_A5
M_B_A4
M_B_A3
M_B_A2
M_B_A1
M_B_A0

13 M_B_DQS_DP[7..0]

M_B_DQS_DP7
M_B_DQS_DP6
M_B_DQS_DP5
M_B_DQS_DP4
M_B_DQS_DP3
M_B_DQS_DP2
M_B_DQS_DP1
M_B_DQS_DP0

13 M_B_DQS_DN[7..0]

M_B_DQS_DN7
M_B_DQS_DN6
M_B_DQS_DN5
M_B_DQS_DN4
M_B_DQS_DN3
M_B_DQS_DN2
M_B_DQS_DN1
M_B_DQS_DN0

13 M_B_BA[1..0]

13 M_B_BG[1..0]

13 M_B_CLK0

13 M_B_CLK#0

13 M_B_CLK1

13 M_B_CLK#1

13 M_B_CS#0

13 M_B_ODT0

13 M_B_ODT1

13 M_B_CKE0

13 M_B_CKE1

13 M_B_CKE2

13 M_B_CKE3

13 M_B_CKE4

13 M_B_CKE5

13 M_B_CKE6

13 M_B_CKE7

13 M_B_CKE8

13 M_B_CKE9

13 M_B_CKE10

13 M_B_CKE11

13 M_B_CKE12

13 M_B_CKE13

13 M_B_CKE14

13 M_B_CKE15

13 M_B_CKE16

13 M_B_CKE17

13 M_B_CKE18

13 M_B_CKE19

13 M_B_CKE20

13 M_B_CKE21

13 M_B_CKE22

13 M_B_CKE23

13 M_B_CKE24

13 M_B_CKE25

13 M_B_CKE26

13 M_B_CKE27

13 M_B_CKE28

13 M_B_CKE29

13 M_B_CKE30

13 M_B_CKE31

13 M_B_CKE32

13 M_B_CKE33

13 M_B_CKE34

13 M_B_CKE35

13 M_B_CKE36

13 M_B_CKE37

13 M_B_CKE38

13 M_B_CKE39

13 M_B_CKE40

13 M_B_CKE41

13 M_B_CKE42

13 M_B_CKE43

13 M_B_CKE44

13 M_B_CKE45

13 M_B_CKE46

13 M_B_CKE47

13 M_B_CKE48

13 M_B_CKE49

13 M_B_CKE50

13 M_B_CKE51

13 M_B_CKE52

13 M_B_CKE53

13 M_B_CKE54

13 M_B_CKE55

13 M_B_CKE56

13 M_B_CKE57

13 M_B_CKE58

13 M_B_CKE59

13 M_B_CKE60

13 M_B_CKE61

13 M_B_CKE62

13 M_B_CKE63

13 M_B_CKE64

13 M_B_CKE65

13 M_B_CKE66

13 M_B_CKE67

13 M_B_CKE68

13 M_B_CKE69

13 M_B_CKE70

13 M_B_CKE71

13 M_B_CKE72

13 M_B_CKE73

13 M_B_CKE74

13 M_B_CKE75

13 M_B_CKE76

13 M_B_CKE77

13 M_B_CKE78

13 M_B_CKE79

13 M_B_CKE80

13 M_B_CKE81

13 M_B_CKE82

13 M_B_CKE83

13 M_B_CKE84

13 M_B_CKE85

13 M_B_CKE86

13 M_B_CKE87

13 M_B_CKE88

13 M_B_CKE89

13 M_B_CKE90

13 M_B_CKE91

13 M_B_CKE92

13 M_B_CKE93

13 M_B_CKE94

13 M_B_CKE95

13 M_B_CKE96

13 M_B_CKE97

13 M_B_CKE98

13 M_B_CKE99

13 M_B_CKE100

13 M_B_CKE101

13 M_B_CKE102

13 M_B_CKE103

13 M_B_CKE104

13 M_B_CKE105

13 M_B_CKE106

13 M_B_CKE107

13 M_B_CKE108

13 M_B_CKE109

13 M_B_CKE110

13 M_B_CKE111

13 M_B_CKE112

13 M_B_CKE113

13 M_B_CKE114

13 M_B_CKE115

13 M_B_CKE116

13 M_B_CKE117

13 M_B_CKE118

13 M_B_CKE119

13 M_B_CKE120

13 M_B_CKE121

13 M_B_CKE122

13 M_B_CKE123

13 M_B_CKE124

13 M_B_CKE125

13 M_B_CKE126

13 M_B_CKE127

13 M_B_CKE128

13 M_B_CKE129

13 M_B_CKE130

13 M_B_CKE131

13 M_B_CKE132

13 M_B_CKE133

13 M_B_CKE134

13 M_B_CKE135

13 M_B_CKE136

13 M_B_CKE137

13 M_B_CKE138

13 M_B_CKE139

13 M_B_CKE140

13 M_B_CKE141

13 M_B_CKE142

13 M_B_CKE143

13 M_B_CKE144

13 M_B_CKE145

13 M_B_CKE146

13 M_B_CKE147

13 M_B_CKE148

13 M_B_CKE149

13 M_B_CKE150

13 M_B_CKE151

13 M_B_CKE152

13 M_B_CKE153

13 M_B_CKE154

13 M_B_CKE155

13 M_B_CKE156

13 M_B_CKE157

13 M_B_CKE158

13 M_B_CKE159

13 M_B_CKE160

13 M_B_CKE161

13 M_B_CKE162

13 M_B_CKE163

13 M_B_CKE164

13 M_B_CKE165

13 M_B_CKE166

13 M_B_CKE167

13 M_B_CKE168

13 M_B_CKE169

13 M_B_CKE170

13 M_B_CKE171

13 M_B_CKE172

13 M_B_CKE173

13 M_B_CKE174

13 M_B_CKE175

13 M_B_CKE176

13 M_B_CKE177

13 M_B_CKE178

13 M_B_CKE179

13 M_B_CKE180

13 M_B_CKE181

13 M_B_CKE182

13 M_B_CKE183

13 M_B_CKE184

13 M_B_CKE185

13 M_B_CKE186

13 M_B_CKE187

13 M_B_CKE188

13 M_B_CKE189

13 M_B_CKE190

13 M_B_CKE191

13 M_B_CKE192

13 M_B_CKE193

13 M_B_CKE194

13 M_B_CKE195

13 M_B_CKE196

13 M_B_CKE197

13 M_B_CKE198

13 M_B_CKE199

13 M_B_CKE200

13 M_B_CKE201

13 M_B_CKE202

13 M_B_CKE203

13 M_B_CKE204

13 M_B_CKE205

13 M_B_CKE206

13 M_B_CKE207

13 M_B_CKE208

13 M_B_CKE209

13 M_B_CKE210

13 M_B_CKE211

13 M_B_CKE212

13 M_B_CKE213

13 M_B_CKE214

13 M_B_CKE215

13 M_B_CKE216

13 M_B_CKE217

13 M_B_CKE218

13 M_B_CKE219

13 M_B_CKE220

13 M_B_CKE221

13 M_B_CKE222

13 M_B_CKE223

13 M_B_CKE224

13 M_B_CKE225

13 M_B_CKE226

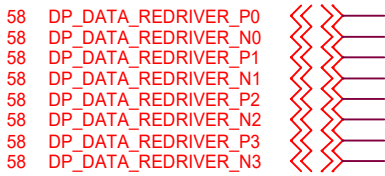
13 M_B_CKE227

13 M_B_CKE228

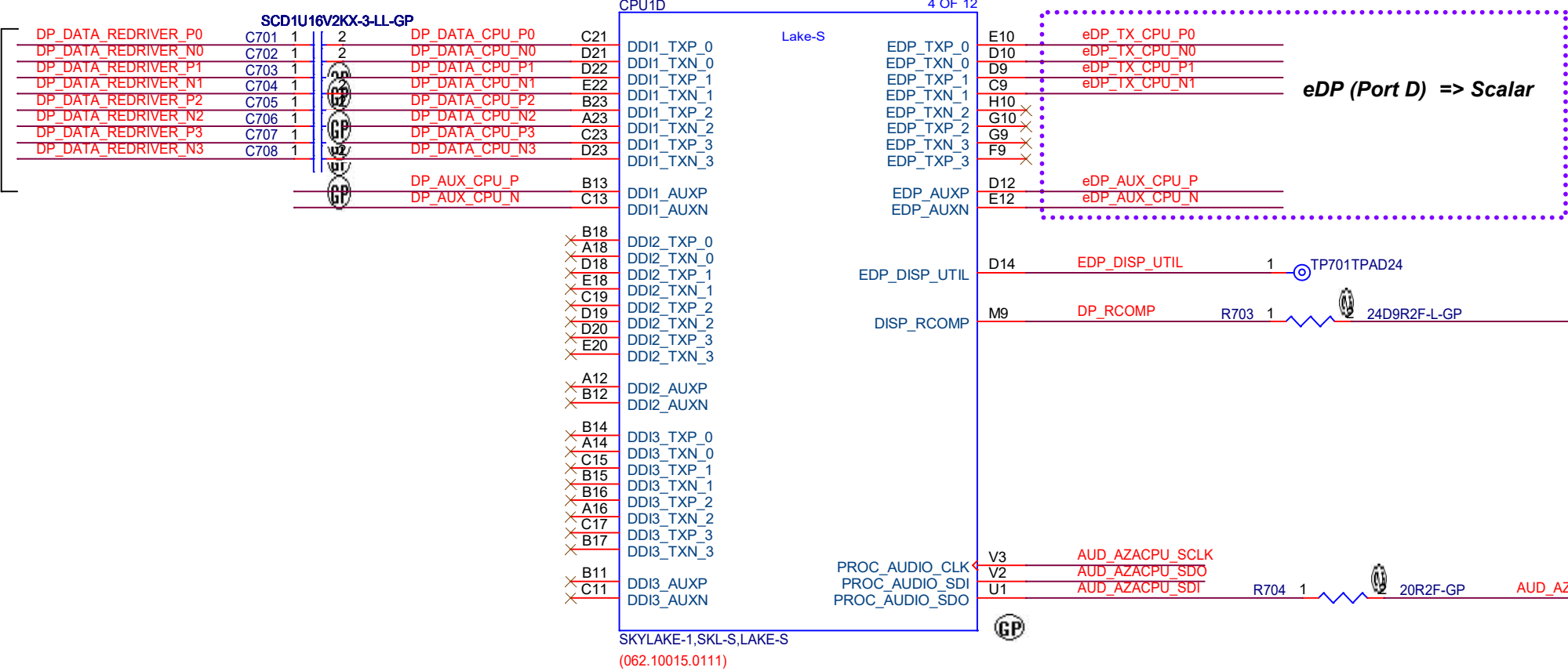
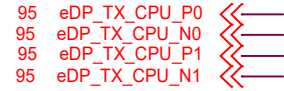
13 M_B_CKE229

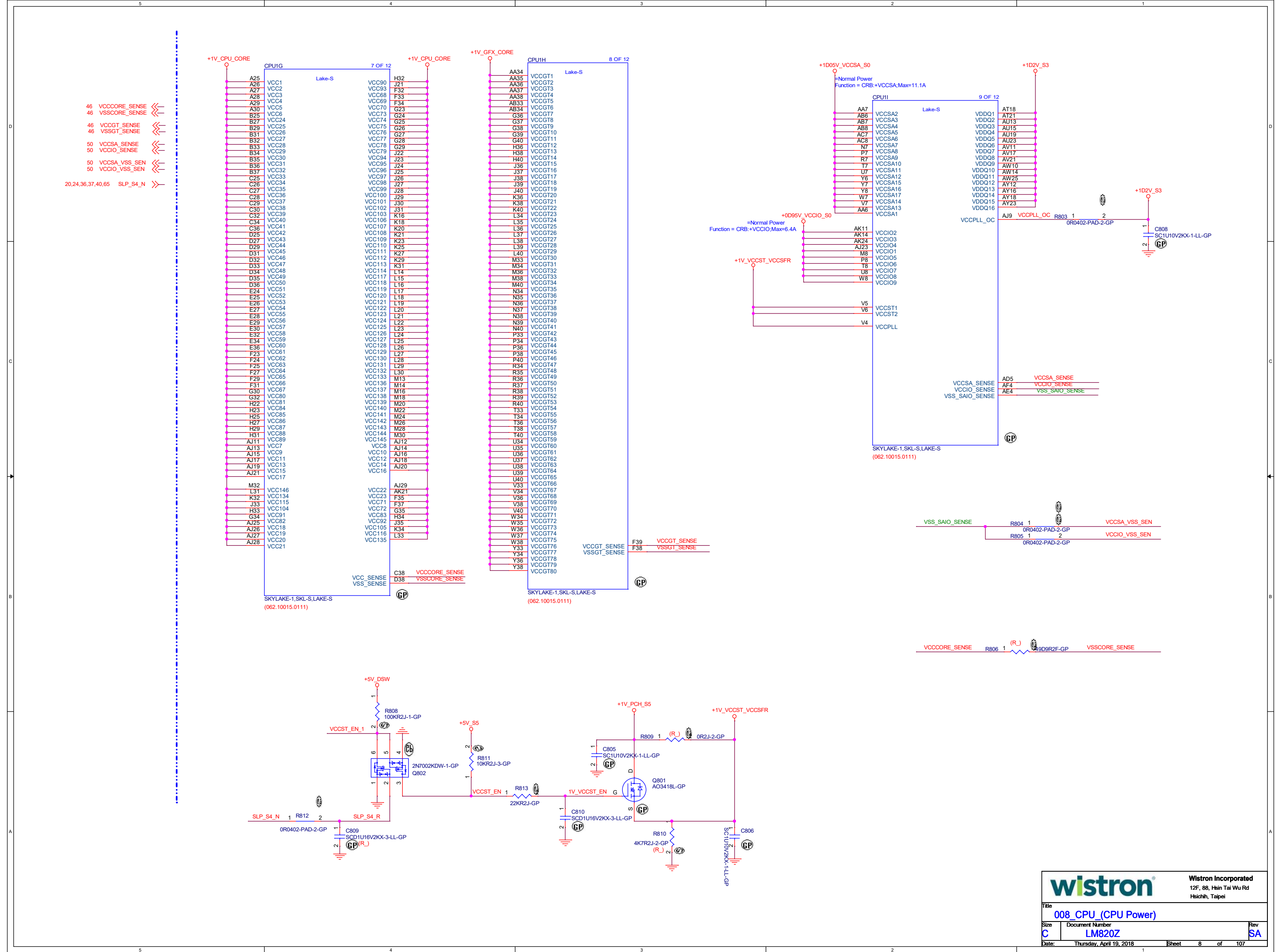
13 M_B_CKE230

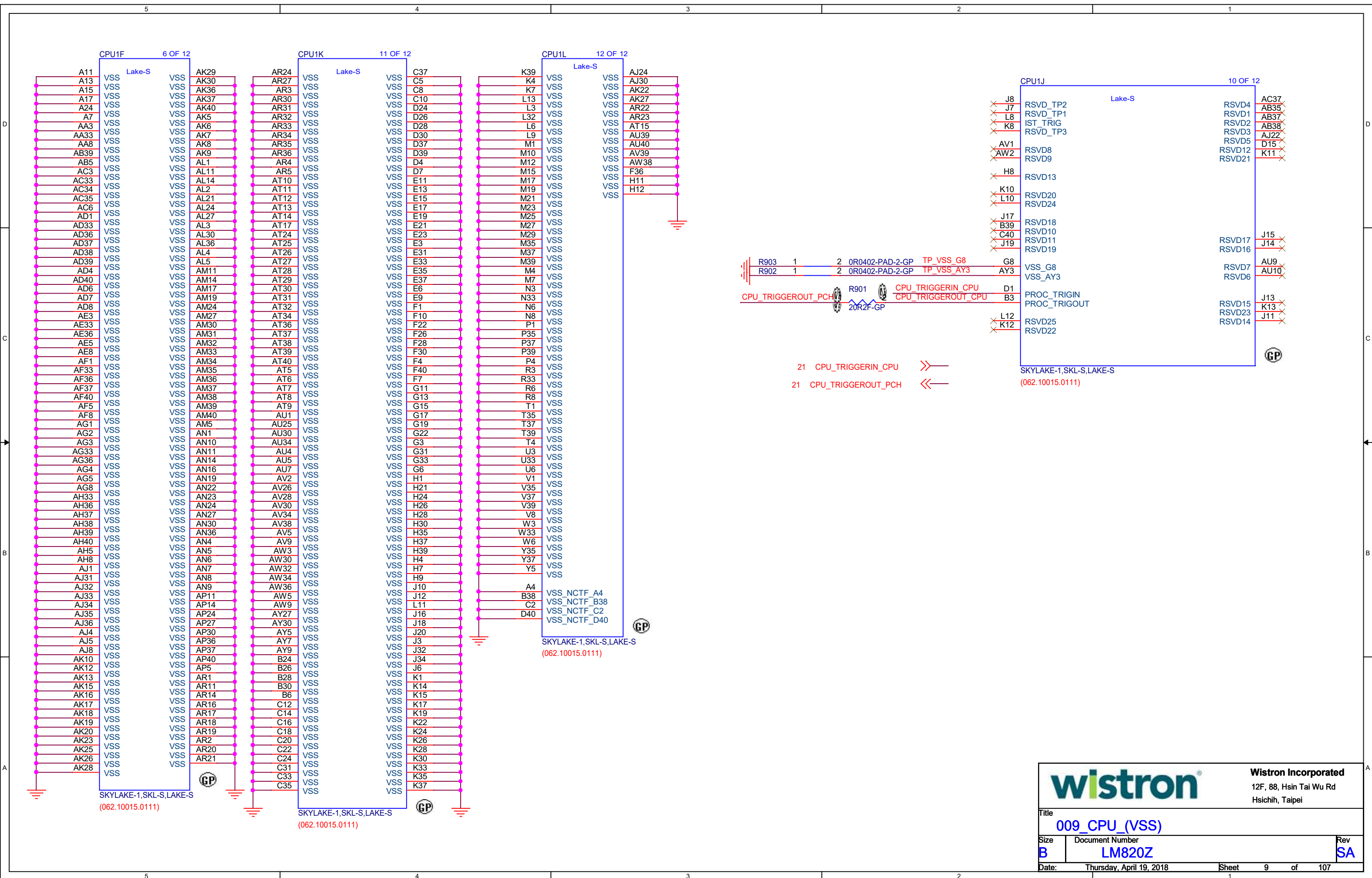
DP OUT

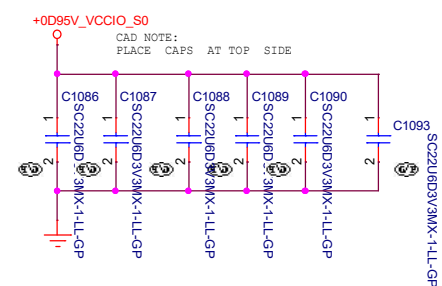
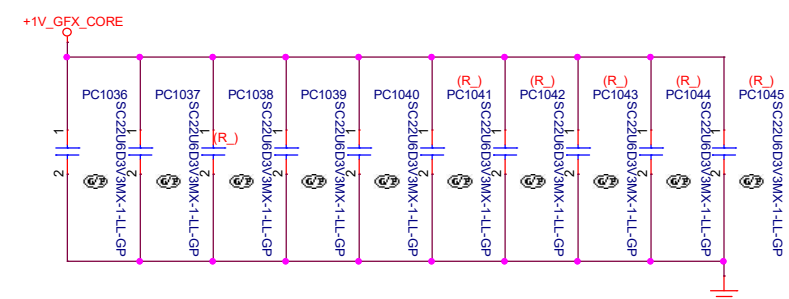
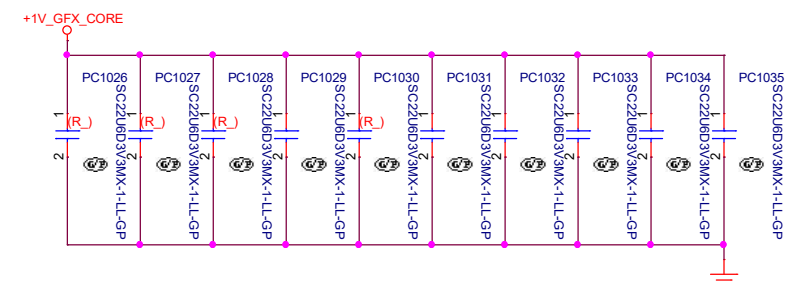
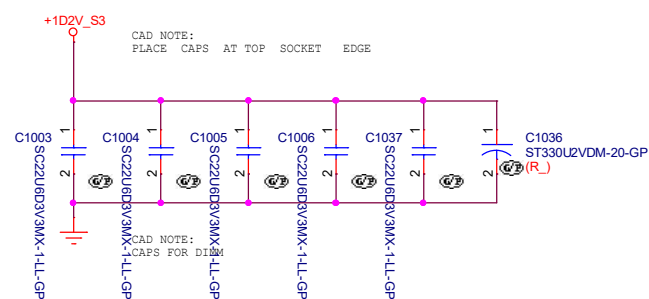
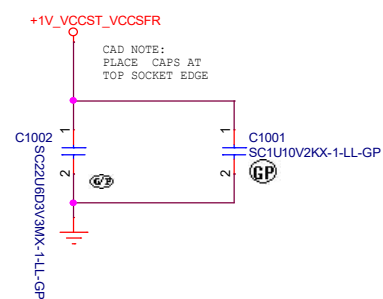
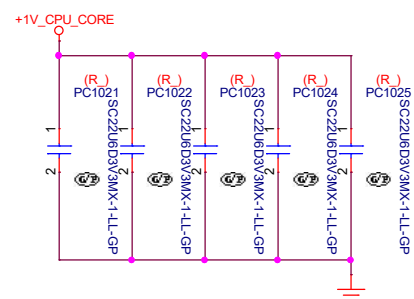
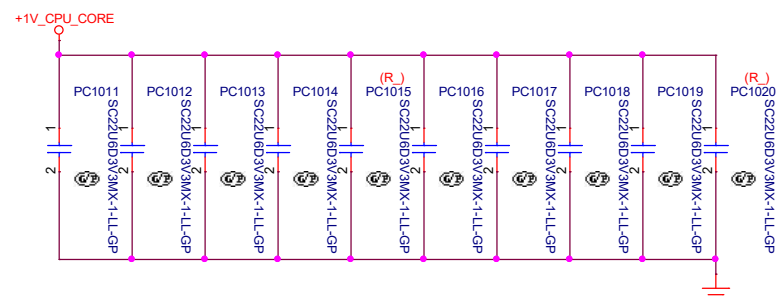
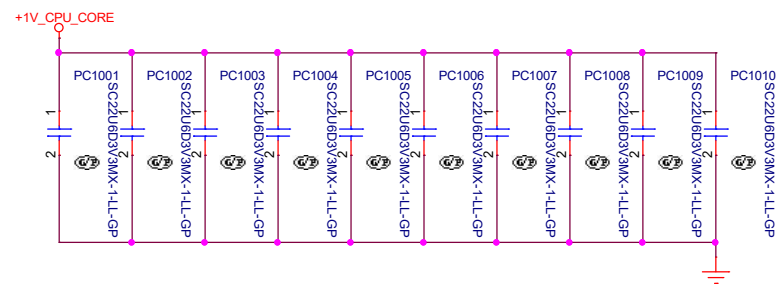


EDP









CHANNEL-A XMM1, A0, H=8mm

DDR DATA

5 M_A_DQ[63..0] <<>
5 M_A_DQS_DN[7..0] <<>
5 M_A_DQS_DP[7..0] <<>

DDR CMD/ADD

5 M_A_A[13..0] <<>
5 M_A_CAS# <<>
5 M_A_WE# <<>
5 M_A_RAS# <<>

DDR CTRL

5 M_A_ODT0 <<>
5 M_A_ODT1 <<>
5 M_A_OKE0 <<>
5 M_A_OKE1 <<>
5 M_A_CS#[1..0] <<>

DDR CLOCK

5 M_A_CLK0 <<>
5 M_A_CLK#0 <<>
5 M_A_CLK1 <<>
5 M_A_CLK#1 <<>

DDR OTHERS

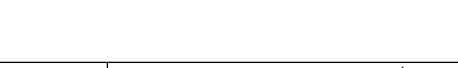
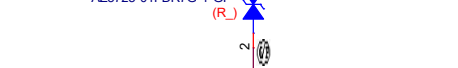
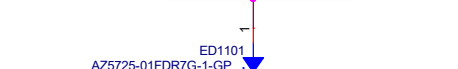
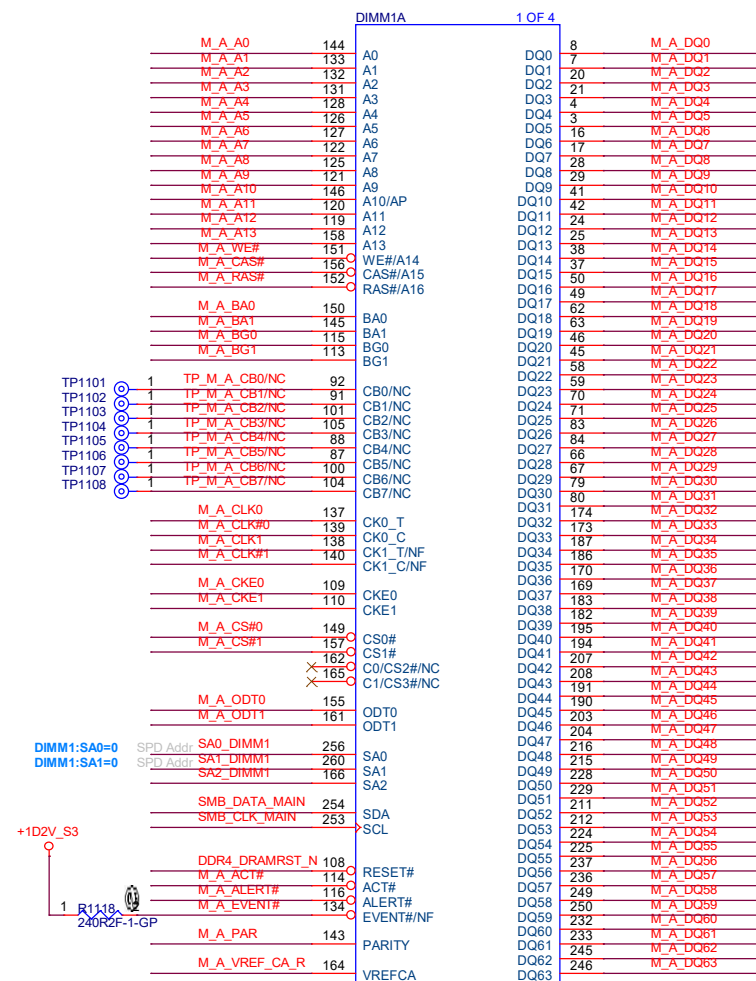
13,20,58,77 SMB_DATA_MAIN <<>
13,20,58,77 SMB_CLK_MAIN <<>

13,20 DDR4_DRAMRST_N <<>
6 M_A_VREF_CA <<>

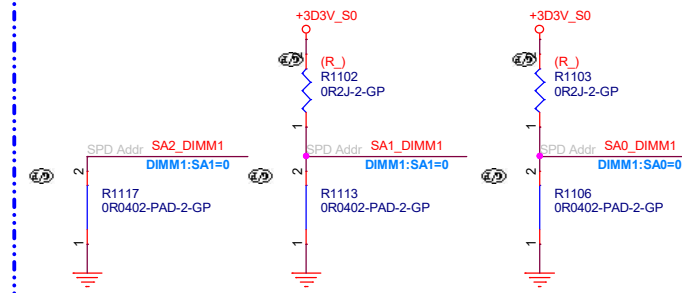
5 M_A_BA[1..0] <<>
5 M_A_BG[1..0] <<>

5 M_A_ACT# <<>

5 M_A_ALERT# <<>
5 M_A_PAR <<>



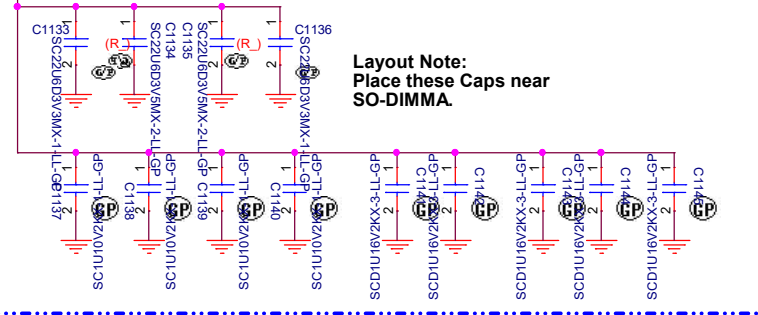
SPD Address of DIMM1



| | |
|---------|---|
| SPD SA2 | 0 |
| SPD SA1 | 0 |
| SPD SA0 | 0 |

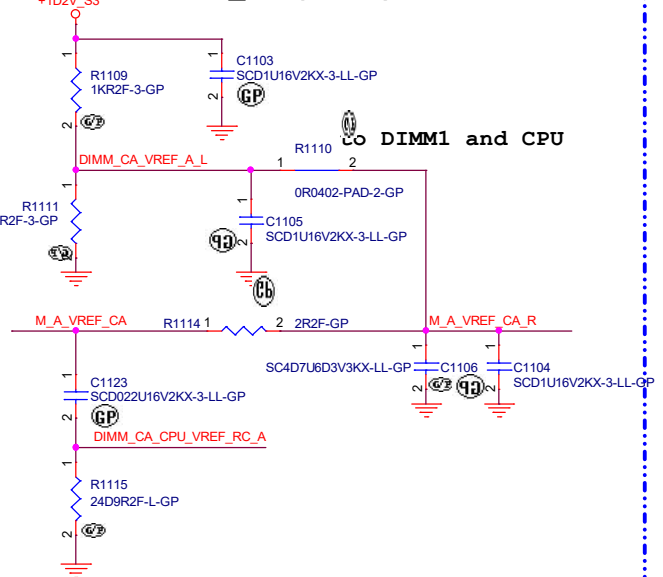
Note:
SA0 DIMM1 = 0, SA1_DIMM1 = 0
SO-DIMMA SPD Address is 0xA0
SO-DIMMA TS Address is 0x30

SODIMM A DECOUPLING



Layout Note:
Place these Caps near
SO-DIMMA.

VREF_CA (Ch. A)



SPD Address Table

| Device | SMBus 0 | 8-bit Address(hex) |
|---------|------------------|--------------------|
| DIMM A0 | Write Addr: 0xA0 | SA1=0; SA0=0 |
| DIMM A1 | Read Addr: 0xA1 | SA1=0; SA0=1 |
| DIMM B0 | Write Addr: 0xA2 | SA1=1; SA0=0 |
| DIMM B1 | Read Addr: 0xA3 | SA1=1; SA0=1 |
| 1 | 0 | 1 |
| 0 | 1 | 0 |
| 0 | 0 | 0 |

Note: 0' 3~7 bit as default



Wistron Incorporated
12F, 88, Hsin Tai Wu Rd
Hsichih, Taipei

D

C

B

A


D

C

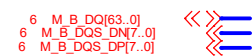
B

A

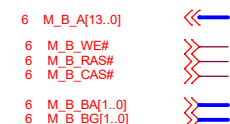
Reserved

| | | | |
|---|---------------------------|---|-----------|
|  | | Wistron Incorporated 12F, 88, Hsin Tai Wu Rd Hsichih, Taipei | |
| Title 012_DDR DIMM_2 (R) | | | |
| Size A | Document Number LM820Z | | Rev SA |
| Date: | Thursday, April 19, 2018 | Sheet | 12 of 107 |

CHANNEL-B DIMM2, A4, H=4mm

[illegible]

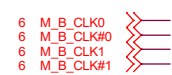
DDR CMD/ADD



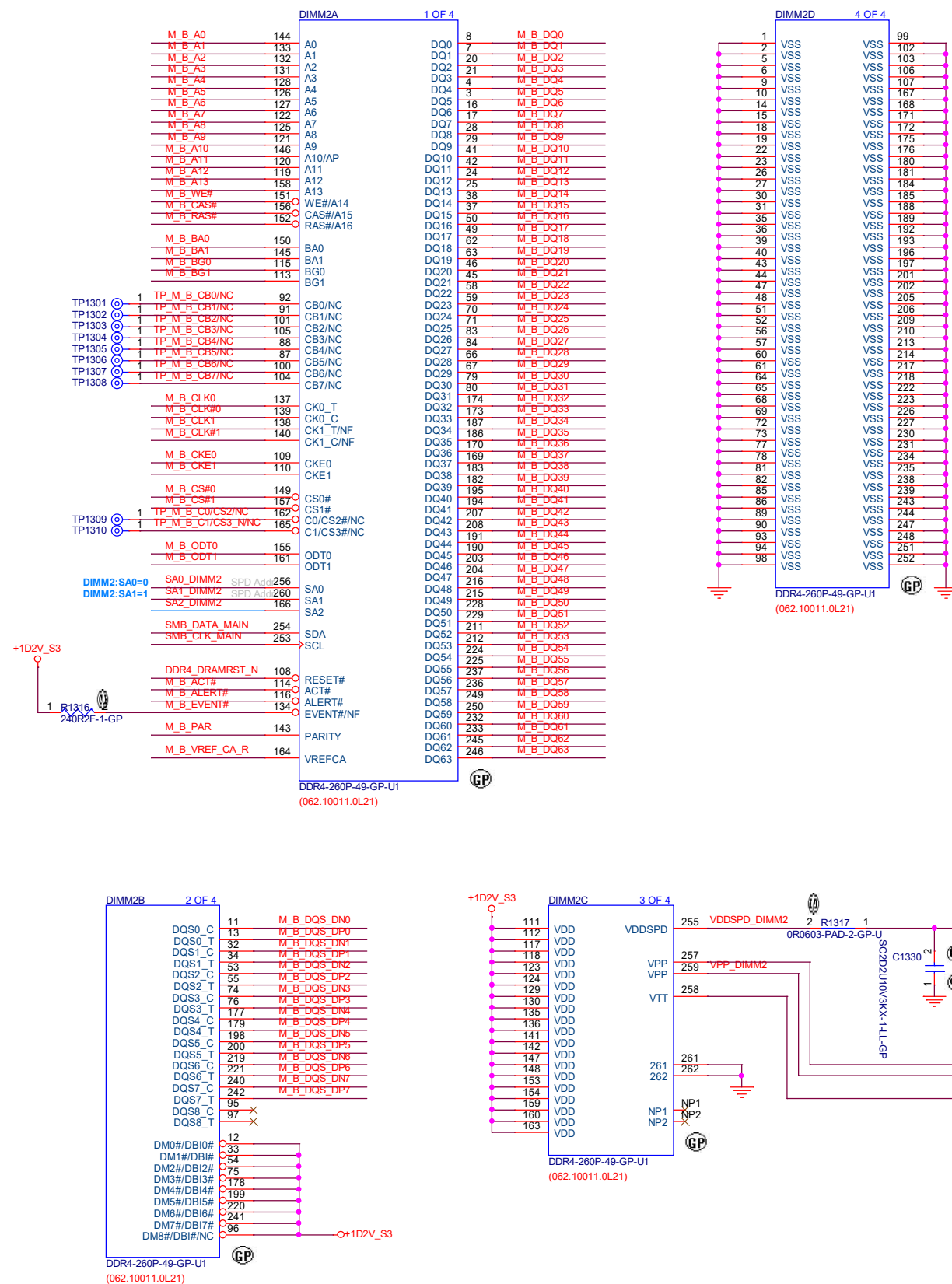
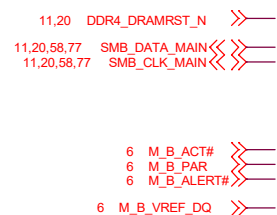
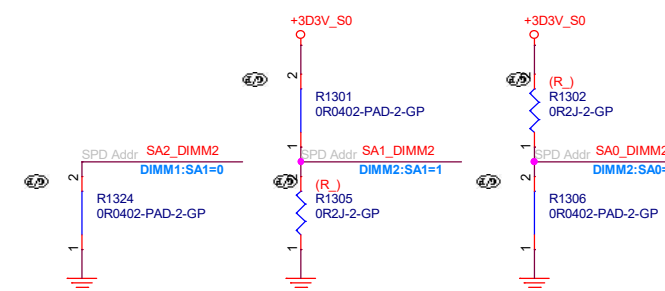
DDR CTRL



DDR CLOCK



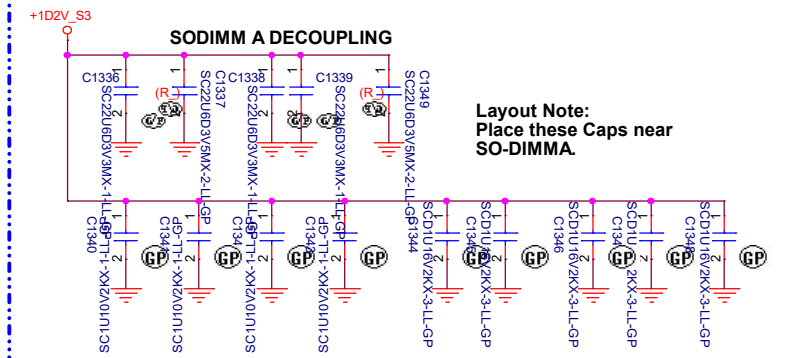
DDR OTHERS

**SPD Address of DIMM2**

| | |
|----------------|---|
| SPD SA2 | 0 |
| SPD SA1 | 1 |
| SPD SA0 | 0 |

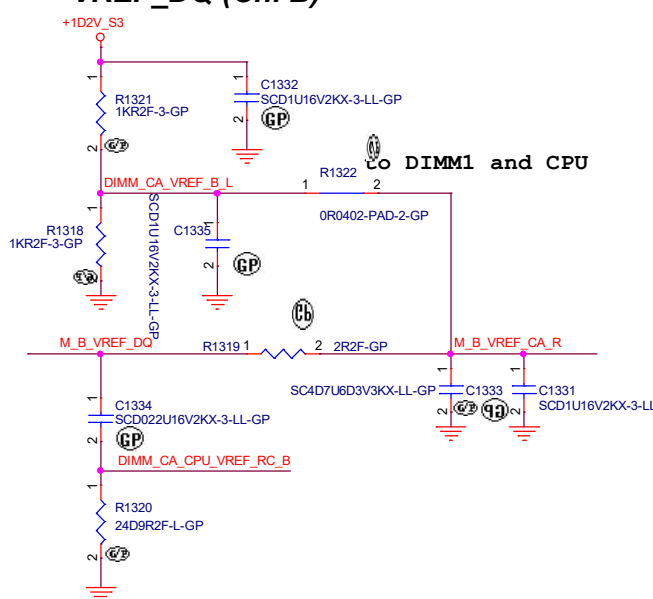
Note:
SA0 DIMM2 = 0, SA1_DIMM2 = 1
SO-DIMMA SPD Address is 0xA4
SO-DIMMA TS Address is 0x34

SODIMM A DECOUPLING



Layout Note:
Place these Caps near
SO-DIMMA.

VREF_DQ (Ch. B)



SPD Address Table

| SMBus 0 | | | |
|-----------------------------|--------------------|--------------|---------|
| Device | 8-bit Address(hex) | | |
| DIMM A0 | Write Addr: 0xA0 | SA1=0; SA0=0 | |
| | Read Addr: 0xA1 | | |
| DIMM A1 | Write Addr: 0xA2 | SA1=0; SA0=1 | |
| | Read Addr: 0xA3 | | |
| DIMM B0 | Write Addr: 0xA4 | SA1=1; SA0=0 | |
| | Read Addr: 0xA5 | | |
| DIMM B1 | Write Addr: 0xA6 | SA1=1; SA0=1 | |
| | Read Addr: 0xA7 | | |
| 1 | 0 | 1 | 0 |
| | | | SA1 SA0 |
| Note: 0' 3~7 bit as default | | | |

D

C

B

A


D

C

B

A

Reserved

| | | | |
|---|---------------------------|---|-----------|
|  | | Wistron Incorporated 12F, 88, Hsin Tai Wu Rd Hsichih, Taipei | |
| Title 014_DDR DIMM_4 (R) | | | |
| Size A | Document Number LM820Z | | Rev SA |
| Date: | Thursday, April 19, 2018 | Sheet | 14 of 107 |

SPIO

22,25,91 SPIO_SI_ROM <<<
22,25,91 SPIO_SO_ROM <<<
25 SPIO_CS0_ROM1 <<<
25,91 SPIO_CLK_ROM <<<
22,25 SPIO_WP_ROM <<<
22,25 SPIO_HOLD_ROM <<<

TPM

22 GPP_H_15 >>>
24,62 PLTRST_N <<<
22 GPP_H_12 >>>
22 LPSS_GSPI1_MOSI >>>
22 LPSS_GSPI0_MOSI >>>
91 SPIO_CS_TPM <<<

61 BT_RF_KILL_R_N <<<

65 PCH_INTRUDER_N >>>
24,25 RTC_DET_N >>>
91 TCM_DET_N >>>
65 CAPTH_DET_N >>>
65 CAM_DET_N >>>
33 CR_DET_N >>>

65 FP_DET_N >>>
65 COMPORT_DET_N >>>
25 CMOS_IN >>>
65 PCH_SATA_LED_TEST >>>
91 SPI_SIRQ# <<<

BOARD ID

16 BOARD_ID_1 >>>
16 BOARD_ID_2 >>>

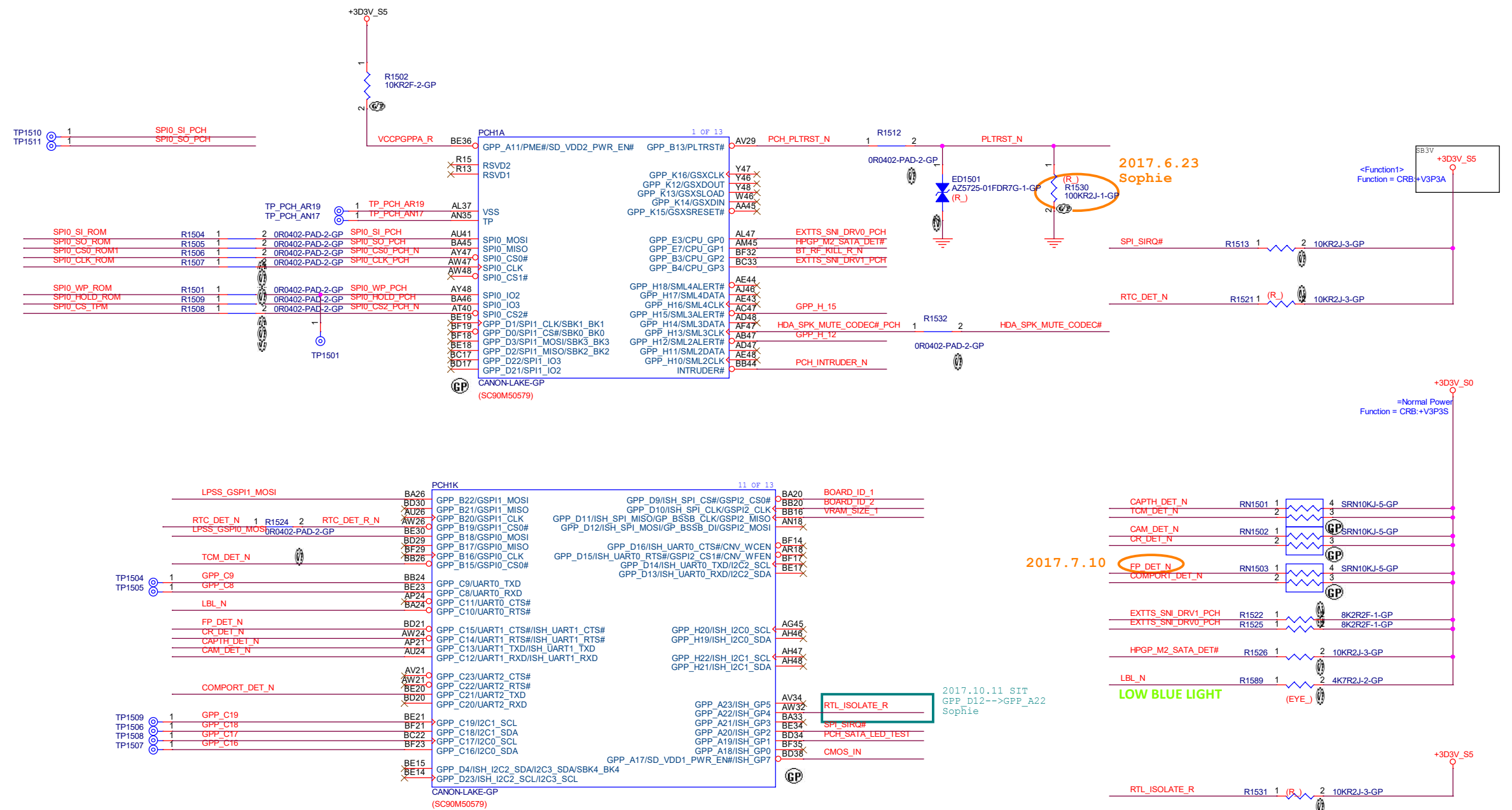
USB DEBUG GPIO

62 HPGP_M2_SATA_DET# >>>

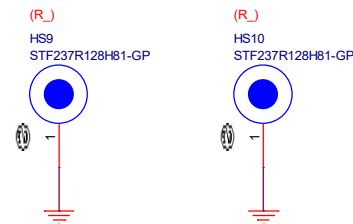
24,65 LBL_N >>>

31 RTL_ISOLATE_R <<<

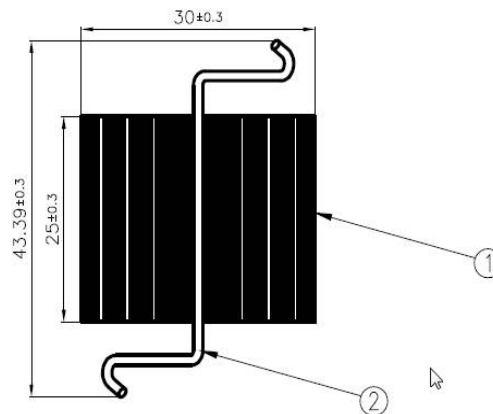
24,27 HDA_SPK_MUTE_CODECH# <<<



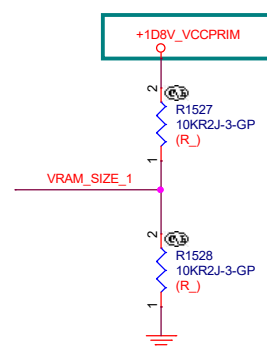
FOR PCH THERMAL SINK



2017.6.14
change PN
Sophie



VRAM SIZE DETECT



2017.10.11 SIT
change to 1.8V
Sophie

wistron

Wistron Incorporated
12F, 88, Hsin Tai Wu Rd
Hsichih, Taipei

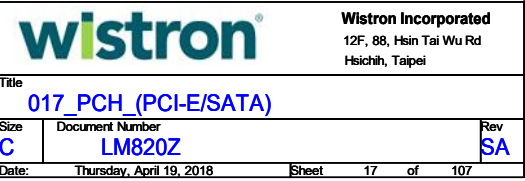
Title
015_PCH_(SPI/UART/I2C)

Size
C

Document Number
LM820Z

Rev
SA

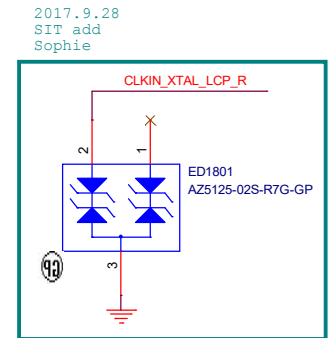
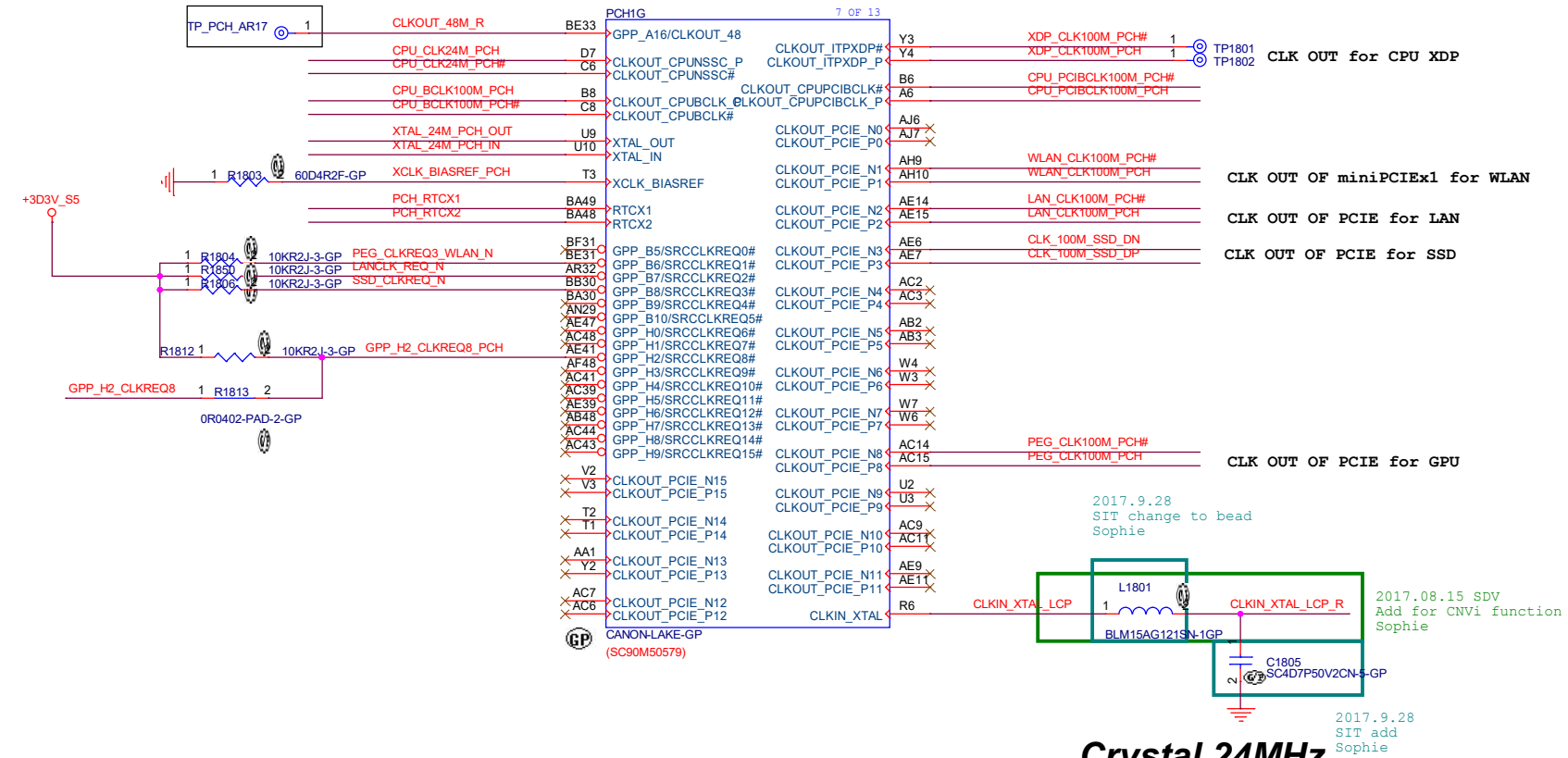
Date: Thursday, April 19, 2018 Sheet 15 of 107



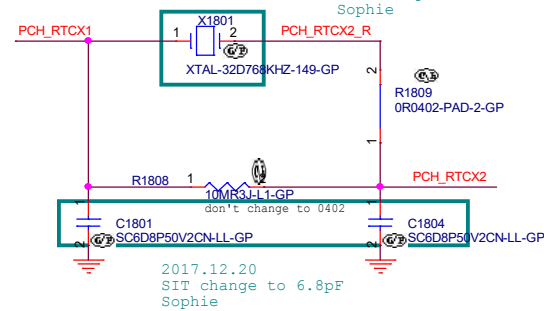
6/21 Delete
CLKOUT_48 is only supported and enabled on SKL-H Server

CLOCK

- 4 CPU_CLK24M_PCH
- 4 CPU_CLK24M_PCH#
- 4 CPU_BCLK100M_PCH
- 4 CPU_BCLK100M_PCH#
- 62 SSD_CLKREQ_N
- 61 PEG_CLKREQ3_WLAN_N
- 31 LANCLK_REQ_N
- 77 GPP_H2_CLKREQ8
- 4 CPU_PCBCLK100M_PCH
- 4 CPU_PCBCLK100M_PCH#
- 61 WLAN_CLK100M_PCH
- 61 WLAN_CLK100M_PCH#
- 31 LAN_CLK100M_PCH
- 31 LAN_CLK100M_PCH#
- 62 CLK_100M_SSD_DP
- 62 CLK_100M_SSD_DN
- 76 PEG_CLK100M_PCH
- 76 PEG_CLK100M_PCH#
- 61 CLKIN_XTAL_LCP_R



Crystal 32.768KHz



Crystal 24MHz

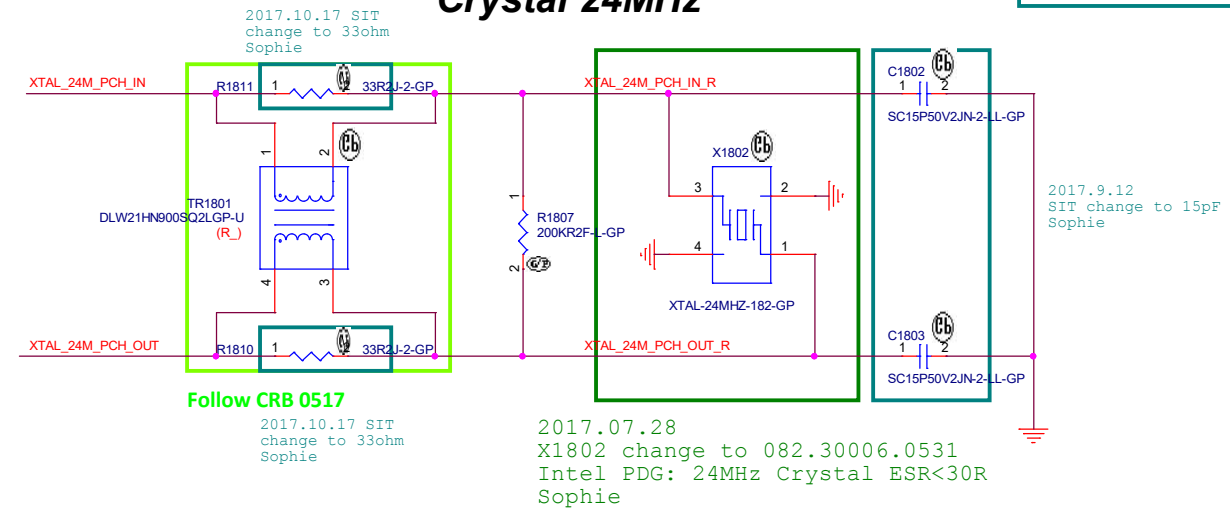
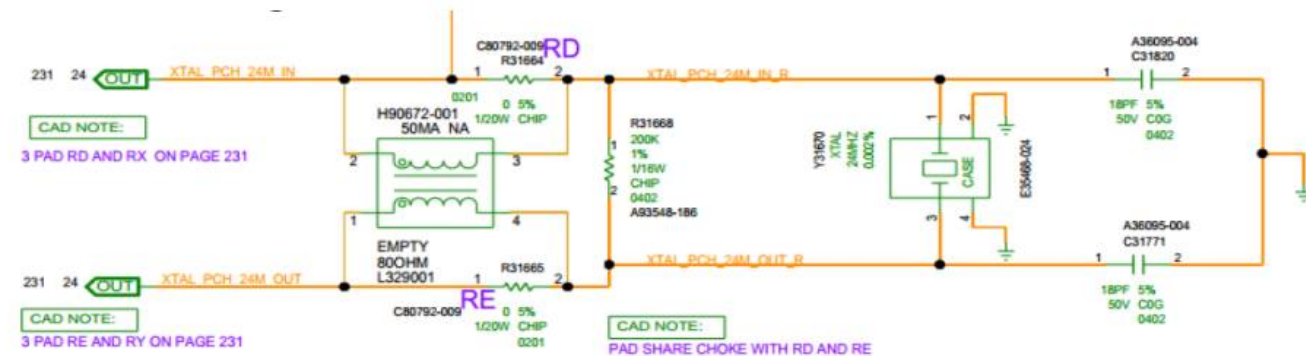
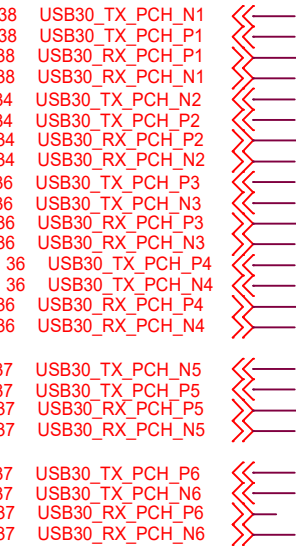


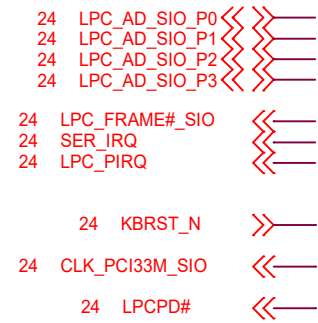
Figure 49-13.Example which shows series resistors and CM Choke for XTAL_IN and XTAL_OUT



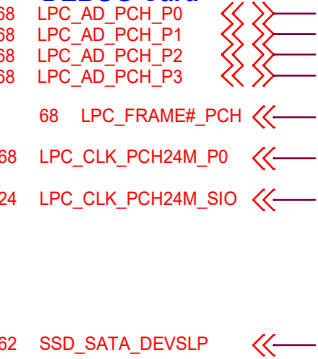
USB3.0X2==>



LPC interface



DEBUG Card



SIDE IO TYPE-C

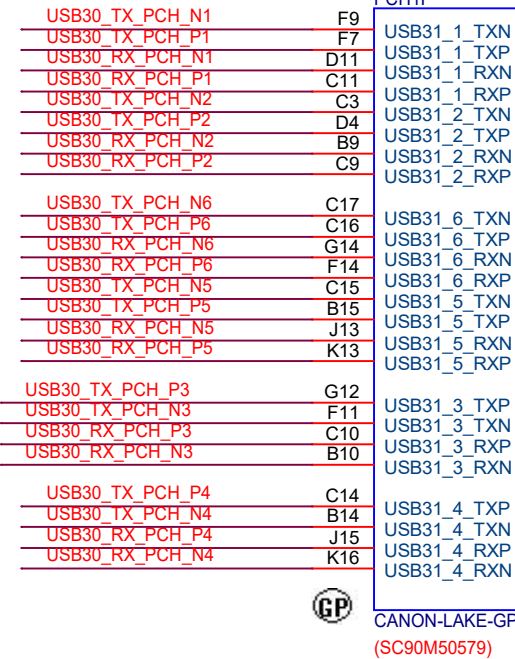
SIDE IO TYPE-A (1)
Charger

REAR IO TYPE-A (USB34)

REAR IO TYPE-A (USB33)

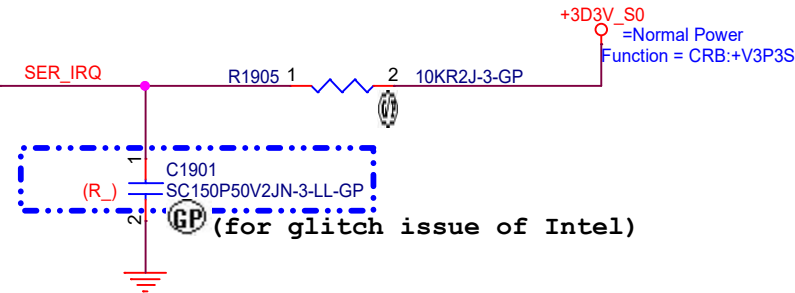
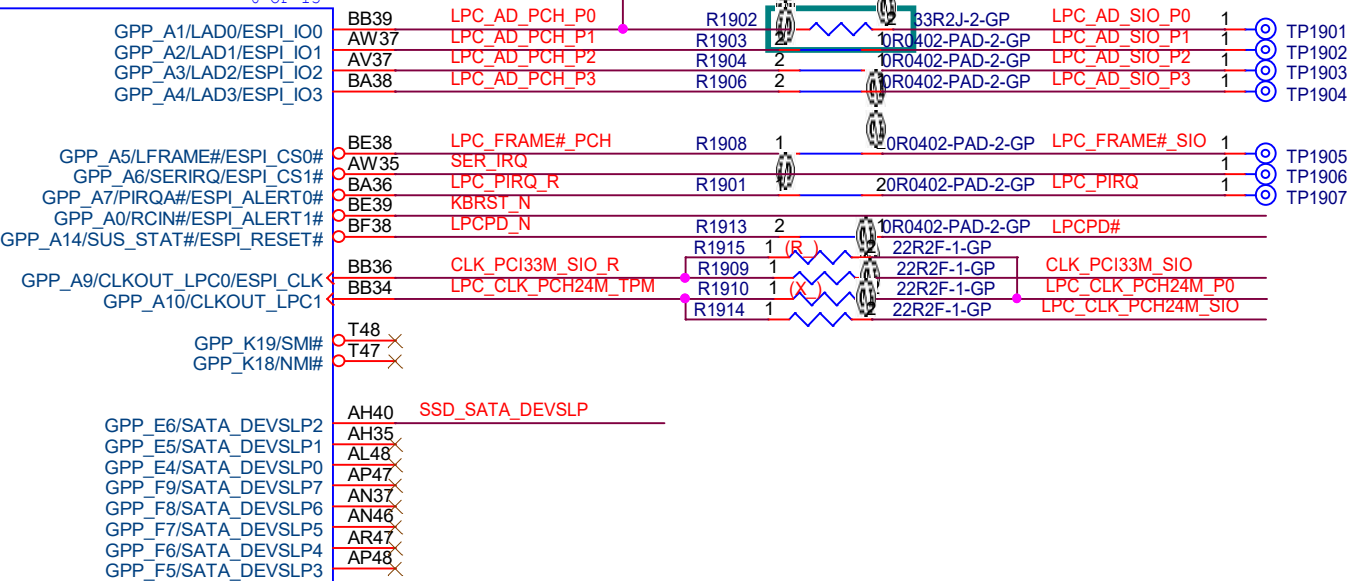
REAR IO TYPE-A (USB31)

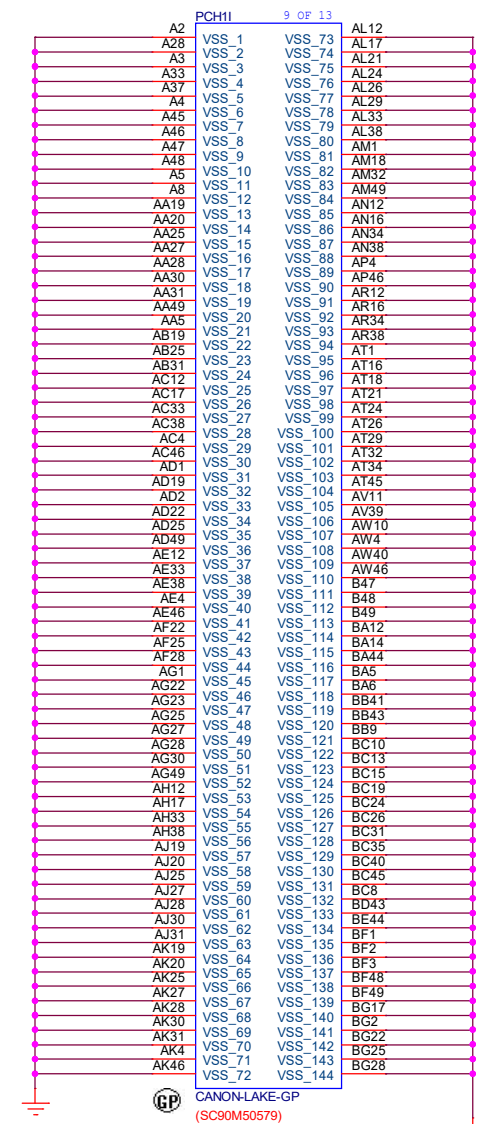
REAR IO TYPE-A (USB32)



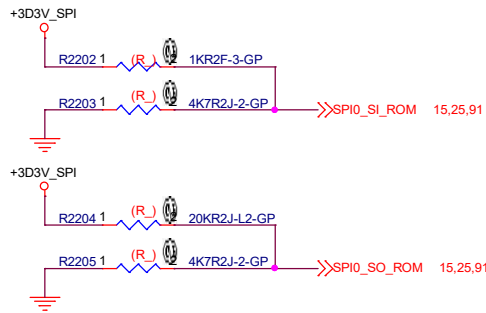
2017.12.8 SIT
add for SI issue
Place close to PCH1
Sophie

2017.12.8 SIT
change to 33ohm
Sophie

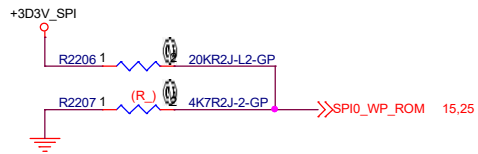




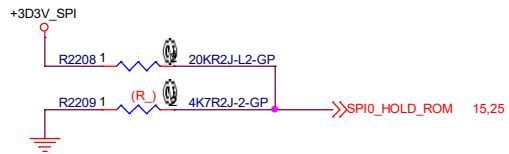
| | | | |
|-----------|----------|------------------------|---|
| SPIO_MOSI | Reserved | Rising edge of RSMRST# | External pull-up is required. Recommend 100K if pulled up to 3.3V or 75K if pulled up to 1.8V. This strap should sample HIGH. There should NOT be any on-board device driving it to opposite direction during strap sampling. |
|-----------|----------|------------------------|---|



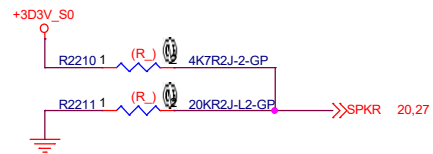
| | | | |
|----------|----------|------------------------|---|
| SPIO_IO2 | Reserved | Rising edge of RSMRST# | External pull-up is required. Recommend 100K if pulled up to 3.3V or 75K if pulled up to 1.8V. This strap should sample HIGH. There should NOT be any on-board device driving it to opposite direction during strap sampling. |
|----------|----------|------------------------|---|



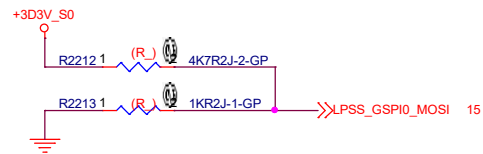
| | | | |
|----------|----------|------------------------|---|
| SPIO_IO3 | Reserved | Rising edge of RSMRST# | External pull-up is required. Recommend 100K if pulled up to 3.3V or 75K if pulled up to 1.8V. This strap should sample HIGH. There should NOT be any on-board device driving it to opposite direction during strap sampling. |
|----------|----------|------------------------|---|



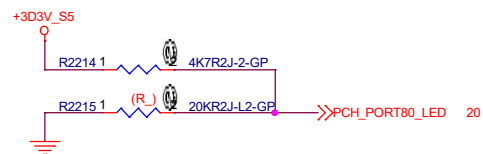
| | | | |
|----------------|-------------------|--------------------------|--|
| GPP_B14 / SPKR | Top Swap Override | Rising edge of PCH_PWR0K | The signal has a weak internal Pull-down. 0 = Disable "Top Swap" mode. (Default) 1 = Enable "Top Swap" mode. This inverts an address on access to SPI and firmware hub, so the processor believes it fetches the alternate boot block instead of the original boot-block. PCH will invert A16 (default) for cycles going to the upper two 64-KB blocks in the FWH or the appropriate address lines (A16, A17, or A18) as selected in Top Swap Block size soft strap. |
|----------------|-------------------|--------------------------|--|



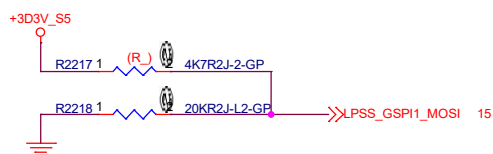
| | | | |
|----------------------|-----------|--------------------------|---|
| GPP_B18 / GSPi0_MOSI | No Reboot | Rising edge of PCH_PWR0K | The signal has a weak internal Pull-down. 0 = Disable "No Reboot" mode. (Default) 1 = Enable "No Reboot" mode (PCH will disable the TCO Timer system reboot feature). This function is useful when running ITP/XDP. |
|----------------------|-----------|--------------------------|---|



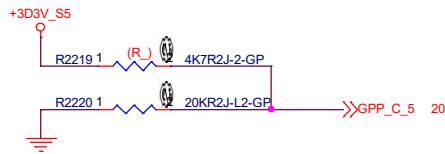
| | | | |
|--------------------|---------------------|------------------------|--|
| GPP_C2 / SMBALERT# | TLS Confidentiality | Rising edge of RSMRST# | This signal has a weak internal Pull-down. 0 = Disable Intel ME Crypto Transport Layer Security (TLS) cipher suite (no confidentiality). (Default) 1 = Enable Intel ME Crypto Transport Layer Security (TLS) cipher suite (with confidentiality). Must be pulled up to support Intel AMT with TLS. |
|--------------------|---------------------|------------------------|--|



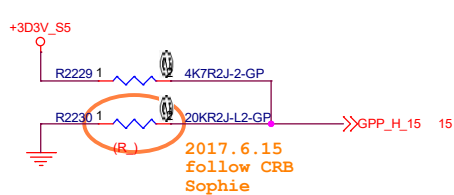
| | | | |
|----------------------|-------------------------|--------------------------|--|
| GPP_B22 / GSPi1_MOSI | Boot BIOS Strap Bit BBS | Rising edge of PCH_PWR0K | This Signal has a weak internal Pull-down. This field determines the destination of accesses to the BIOS memory range. Also controllable using Boot BIOS Destination bit (Bus0, Device31, Function0, offset DCh, bit 6). Bit 6 Boot BIOS Destination 0 = SPI (Default) 1 = LPC |
|----------------------|-------------------------|--------------------------|--|



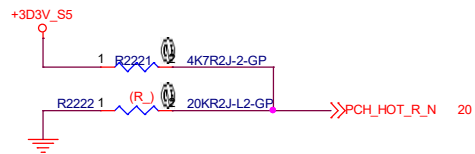
| | | | |
|---------------------|-------------|------------------------|---|
| GPP_C5 / SML0ALERT# | eSPI or LPC | Rising edge of RSMRST# | This signal has a weak internal Pull-down. 0 = LPC is selected (for EC). (Default) 1 = eSPI is selected (for EC). |
|---------------------|-------------|------------------------|---|



| | | | |
|----------------------|----------|------------------------|---|
| GPP_H15 / SML3ALERT# | Reserved | Rising edge of RSMRST# | External pull-up is required. Recommend 100K if pulled up to 3.3V or 75K if pulled up to 1.8V. This strap should sample HIGH. There should NOT be any on-board device driving it to opposite direction during strap sampling. |
|----------------------|----------|------------------------|---|

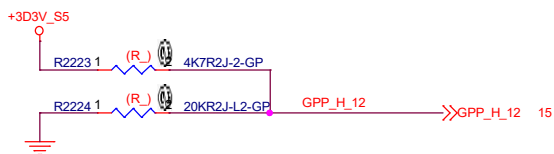


| | | | |
|--------------------------------|----------|------------------------|---|
| GPP_B23 / SML1ALERT# / PCHHOT# | Reserved | Rising edge of RSMRST# | This signal has an internal Pull-down. External pull-up is required. This strap should sample HIGH. There should NOT be any on-board device driving it to opposite direction during strap sampling. |
|--------------------------------|----------|------------------------|---|



| | | | |
|--------------------|------------------------------------|--------------------------|---|
| HDA_SDO / I2S0_TXD | Flash Descriptor Security Override | Rising edge of PCH_PWR0K | This signal has a weak internal Pull-down. 0 = Enable security measures defined in the Flash Descriptor. (Default) 1 = Disable Flash Descriptor Security (override). This strap should only be asserted high using external Pull-up in manufacturing/debug environments ONLY. |
| ME DISABLE JUMPER | | | |

| | | | |
|----------------------|-------------------------|------------------------|--|
| GPP_H12 / SML2ALERT# | eSPI Flash Sharing Mode | Rising edge of RSMRST# | This signal has a weak internal pull-down. 0 = Master Attached Flash Sharing (MAFS) enabled (Default) 1 = Slave Attached Flash Sharing (SAFS) enabled. |
|----------------------|-------------------------|------------------------|--|



| | | | |
|------------------------|-------------------------|--------------------------|--|
| GPP_I6 / DDPB_CTRLDATA | Display Port B Detected | Rising edge of PCH_PWR0K | This signal has a weak internal Pull-down. 0 = Port B is not detected. (Default) 1 = Port B is detected. |
|------------------------|-------------------------|--------------------------|--|



| | | | |
|-----------------------|-------------------------|--------------------------|--|
| GPP_I8 / DDP_CTRLDATA | Display Port C Detected | Rising edge of PCH_PWR0K | This signal has a weak internal Pull-down. 0 = Port C is not detected. (Default) 1 = Port C is detected. |
|-----------------------|-------------------------|--------------------------|--|



| | | | |
|-------------------------|-------------------------|--------------------------|--|
| GPP_I10 / DDPD_CTRLDATA | Display Port D Detected | Rising edge of PCH_PWR0K | This signal has a weak internal pull-down. 0 = Port D is not detected. (Default) 1 = Port D is detected. |
|-------------------------|-------------------------|--------------------------|--|



| | | | |
|---------|-------------------------|--------------------------|--|
| GPP_F23 | Display Port F Detected | Rising edge of PCH_PWR0K | This signal has a weak internal pull-down. 0 = Port F is not detected. (Default) 1 = Port F is detected. |
|---------|-------------------------|--------------------------|--|

PCIVAUX power control

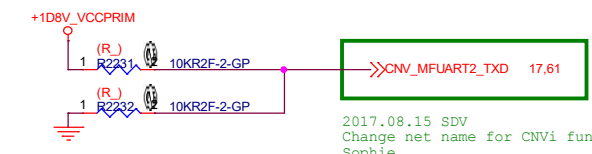
| | | | |
|----------------------------------|-----------------------|------------------------|---|
| GPP_J4 / CNV_BRI_DT / UART0_RTS# | XTAL Frequency Select | Rising edge of RSMRST# | This signal has a weak internal pull-down. 0 = 38.4/19.2MHz XTAL frequency selected. (Default) 1 = 24MHz XTAL frequency selected. |
|----------------------------------|-----------------------|------------------------|---|



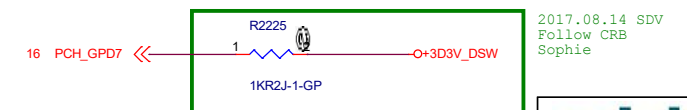
| | | | |
|---------------------------------|---------------------|------------------------|--|
| GPP_J6 / CNV_RGI_DT / UART0_TXD | M.2 CNV Mode Select | Rising edge of RSMRST# | An external pull-up or pull-down is required. 0 = Integrated CNVi enable. 1 = Integrated CNVi disable. |
|---------------------------------|---------------------|------------------------|--|



| | | | |
|--------|--------------|------------------------|--|
| GPP_J9 | 1.8V VCCPSPI | Rising edge of RSMRST# | The signal has a weak internal pull-down 0 = VCCPSPI is connected to 3.3V rail 1 = VCCPSPI is connected to 1.8V rail |
|--------|--------------|------------------------|--|



| | | | |
|------|----------|--------------------------|---|
| GPD7 | Reserved | Rising edge of DSW_PWR0K | External pull-up is required. Recommend 100K. This strap should sample HIGH. There should NOT be any on-board device driving it to opposite direction during strap sampling |
|------|----------|--------------------------|---|



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Hsichih, Taipei

Title
022_PCH_Strap

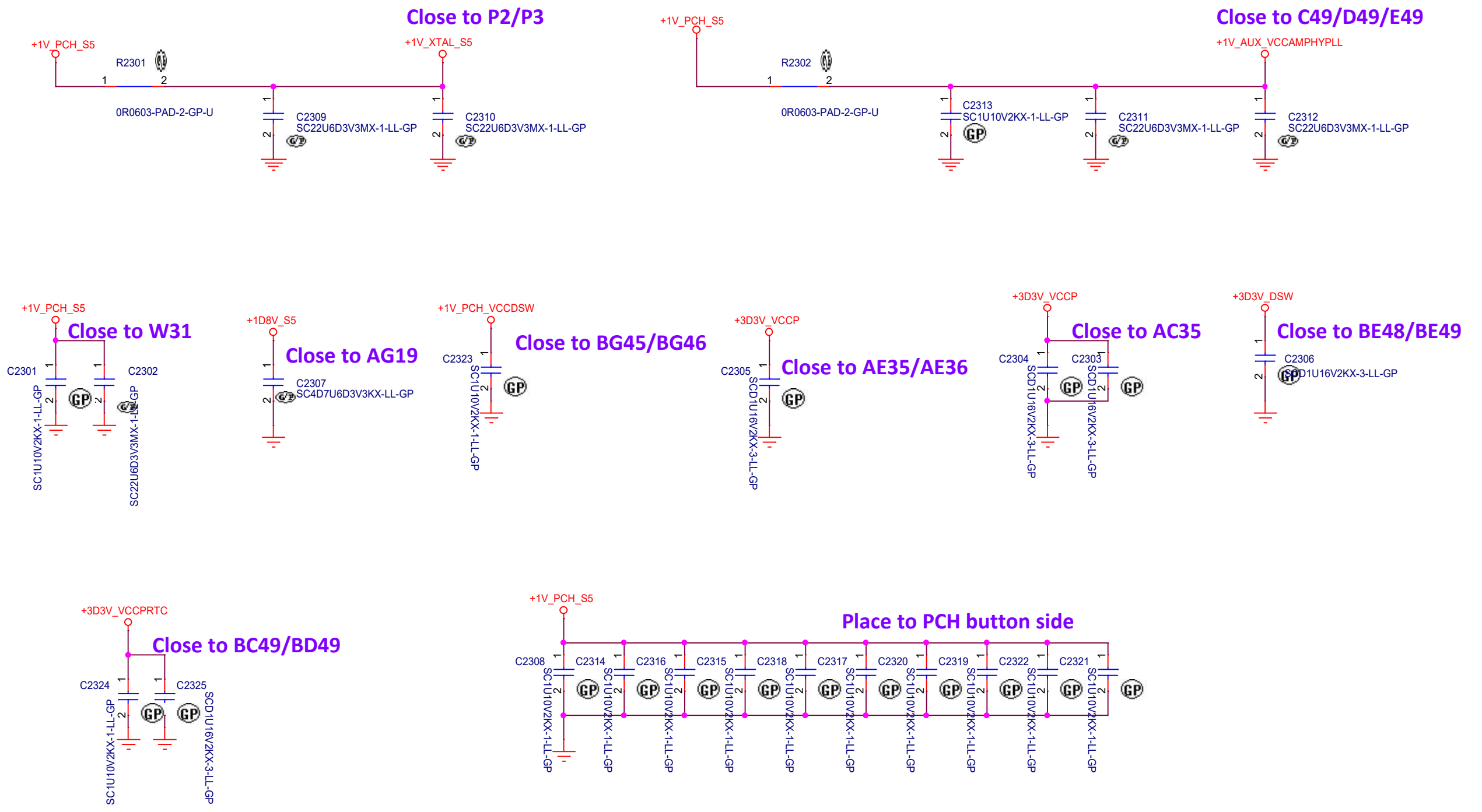
Size Document Number
Cuspm LM820Z

Date: Thursday, April 19, 2018

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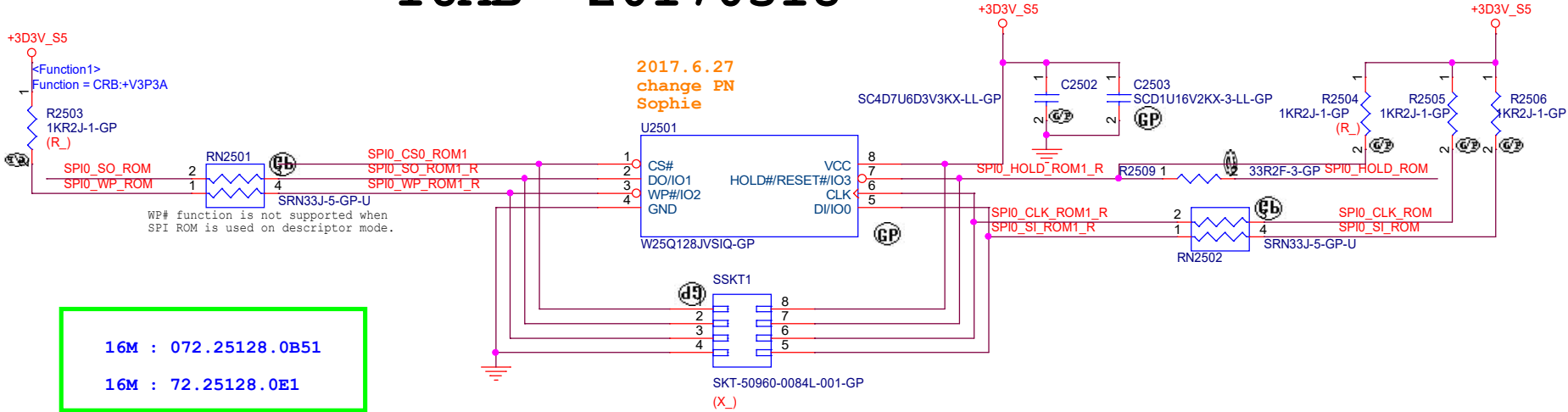
Rev
SA

Follow CRB page132
0509



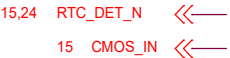
PCH SPI ROM

16MB 20170518



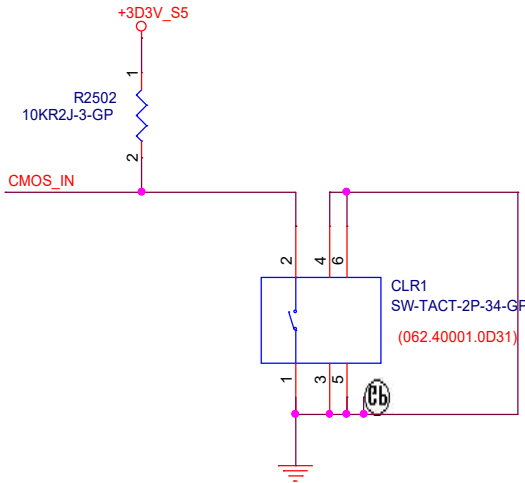
SPI socket mount in SA stage

SPI0 ROM

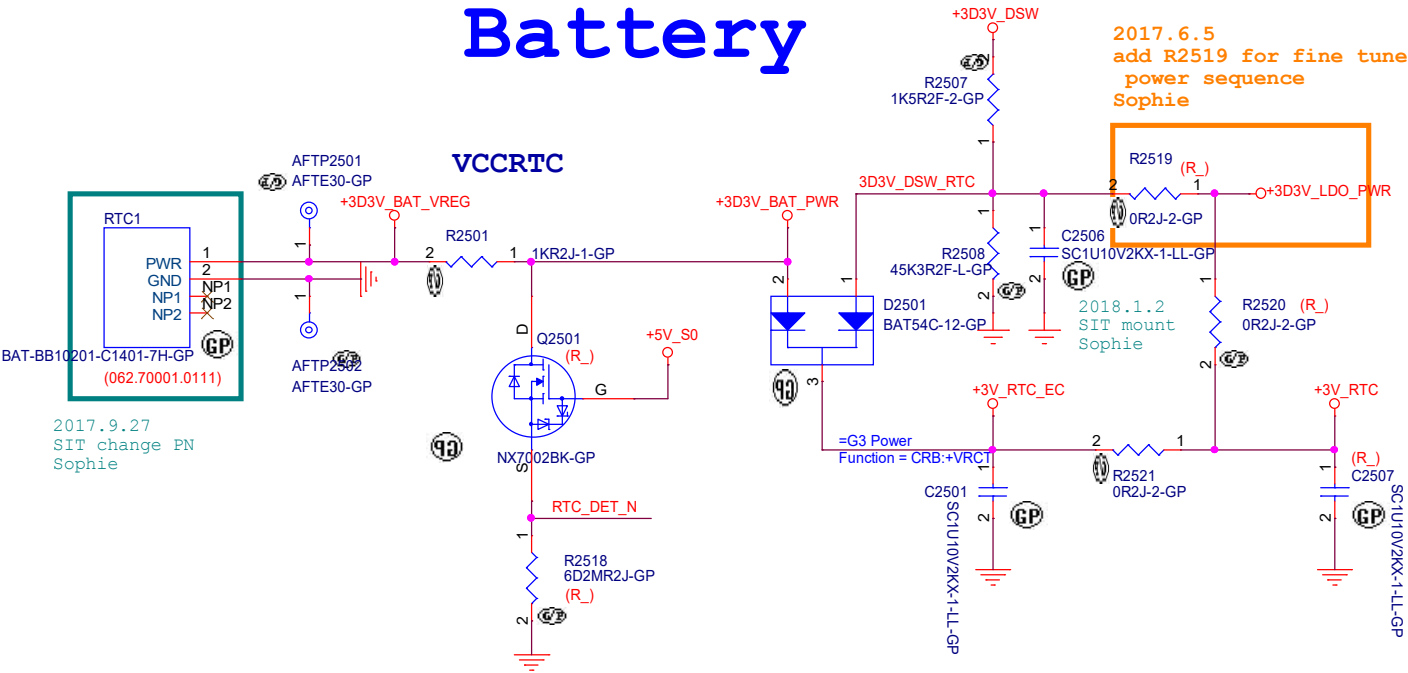


BOOT BLOCK

| | |
|-----|------------------|
| 1-2 | NORMAL (DEFAULT) |
| 2-3 | BOOT BLOCK |



Battery



wistron

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Hsichih, Taipei

Title
025_SPI&RTC

Size Document Number

Custom LM820Z

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Rev

SA



REALTEK

HD LINK

20 HDA_BITCLK_CODEC
20 HDA_SDIN_PCH
20 HDA_SYNC_CODEC
20 HDA_RST#_CODEC
20 HDA_SDOOUT_PCH_R

65 DMIC_DATA
65 DMIC_CLK

29 SPKR_L+
29 SPKR_L-
29 SPKR_R+
29 SPKR_R-

29 SLEEVE
29 MIC2-VREF0
29 RING2
29 HPOUT-L
29 HPOUT-R

29 LINE1-R
29 LINE1-L

29 LINE1-VREF0-L
29 LINE1-VREF0-R
29 HPOUT_ID

MIC mute from ECIO

15,24 HDA_SPK_MUTE_CODEC#
24 HDA_MIC_MUTE_CODEC
65 HDA_MIC_LED_CODEC

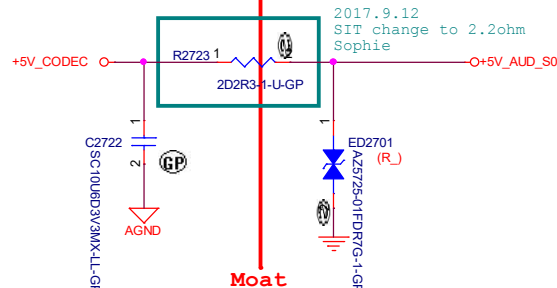
Buzzer from PCH

20,22 SPKR

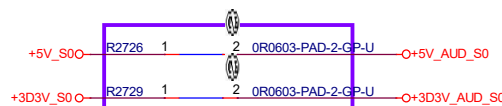
Analog
Digital

speaker traces width >40mil when 2W4ohm speaker

ANALOG DIGITAL



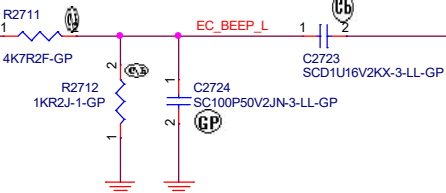
In order to prevent the built-in LDO damaged from over-voltage on +5VSYS or Standby power line, we suggested using this Voltage suppressing device.



2018.3.29 SVT
change to short pad
Sophie

Place beep circuit nearby codec.

PCH Beep



ALC233

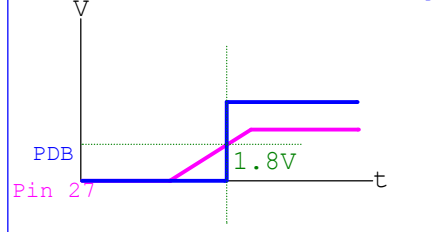
(Include Thermal pad)

QFN48 (6x6)

ALC233-CG-GR-L
(071.00233.0005)

(R) --- ALC233 / ALC233VB
0 Ω --- ALC283

Vref(Pin 28)/PDB(Pin47) timing



| State | HDA_MIC_LED_CODEC (GPIO2/PIN48) |
|-------|---------------------------------|
| 0 | Microphone Un-mute |
| 1 | Microphone mute |

| State | HDA_MIC_MUTE_CODEC (Q2703 Gate) |
|-------|---------------------------------|
| 0 | Microphone Un-mute |
| 1 | Microphone mute |

R2703 For ALC233 mount
For ALC233VB2 set as NC

R2715 (64.39225.6DL) (39.2K) for
ALC233/ACL283 use

place close to pin 9

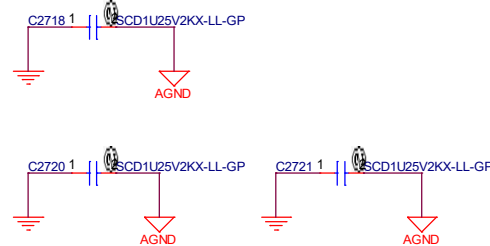
Digital_ground Analog_ground

Digital_ground Analog_ground

Near AVDD1 and AVDD2 power source input

Digital_ground Analog_ground

Tied at one point only under
Codec or near the Codec



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Hsichih, Taipei

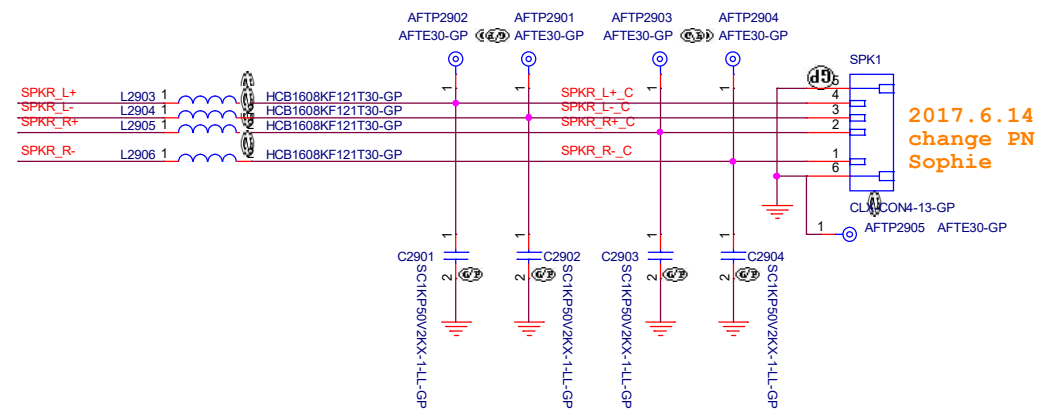
027_Audio Codec (ALC233)

Document Number
LM820Z

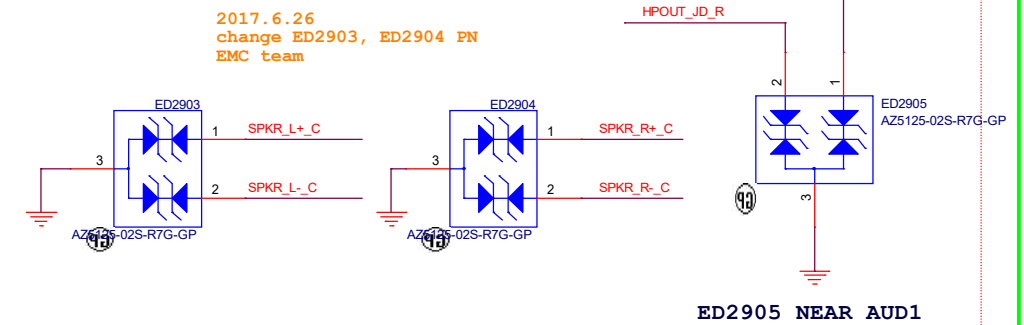
Date: Thursday, April 19, 2018 Sheet 27 of 107

Reserved

Internal Speaker x 2

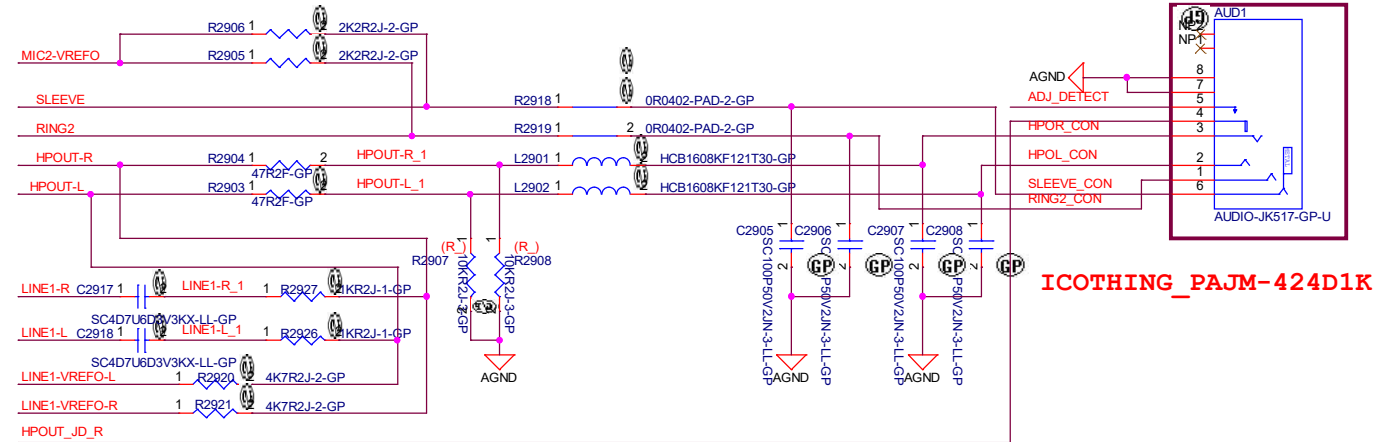


ESD



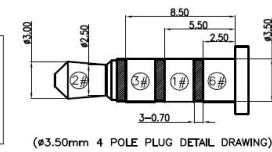
UAJ Headset

(ALC233 supported iPhone/Nokia headset, Headphone)



Pin Define:
Pin1: Ring2
Pin2: HP_L
Pin3: HP_R
Pin4: JD
Pin5: AGND
Pin6: Sleeve
Pin7: GND
Pin8: GND

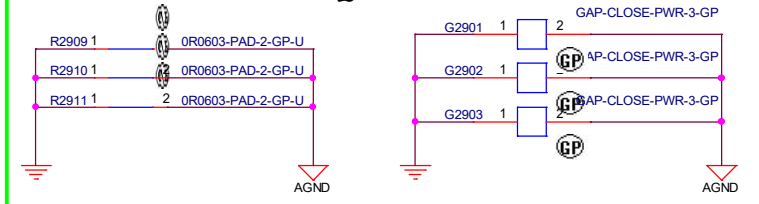
B.COLOR
1.BLACK



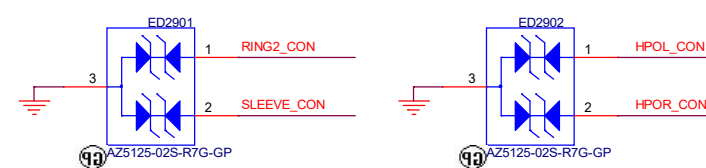
4-pin 3.5mm Headset Connector Pinout



EMC REQUEST



ESD



Nokia, Lenovo mobile

| Pin Number | Pin Name | Description |
|------------|----------|-----------------|
| 1 | Tip | Left Audio Out |
| 2 | Ring-1 | Right Audio Out |
| 3 | Ring-2 | Microphone |
| 4 | Sleeve | Ground / Common |

iPhone, Samsung, Blackberry, HTC

| Pin Number | Pin Name | Description |
|------------|----------|-----------------|
| 1 | Tip | Left Audio Out |
| 2 | Ring-1 | Right Audio Out |
| 3 | Ring-2 | Ground / Common |
| 4 | Sleeve | Microphone |

wistron

Wistron Incorporated
12F, 88, Hsin Tai Wu Rd
Hsichih, Taipei

Title
029_Audio Jack (MIC/SPEA) (1/2)

Size
C

Document Number
LM820Z

Rev
SA

Date: Thursday, April 19, 2018 Sheet 29 of 107

2017.6.26
change ED2901, ED2902 PN
EMC team

D

C

B

A


D

C

B

A

Reserved

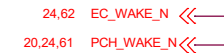
| | | | |
|---|---------------------------|---|-----------------|
|  | | Wistron Incorporated 12F, 88, Hsin Tai Wu Rd Hsichih, Taipei | |
| Title 030_Audio Jack_(function) (R) | | | |
| Size A | Document Number LM820Z | | Rev SA |
| Date: | Thursday, April 19, 2018 | | Sheet 30 of 107 |



LAN CLOCK



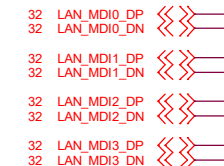
WAKE ON LAN



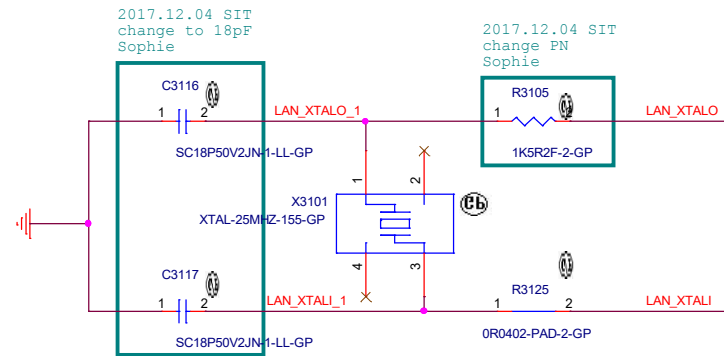
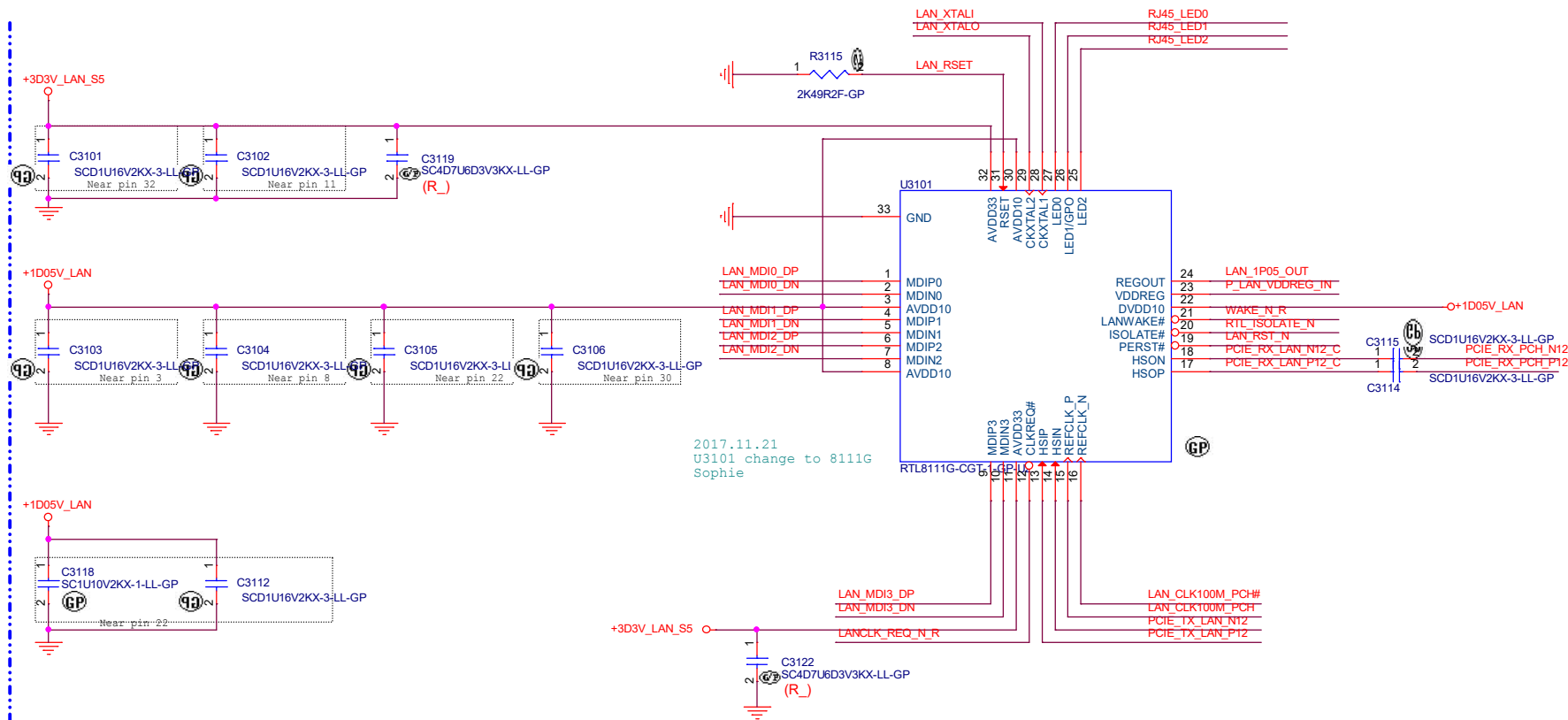
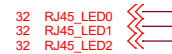
LAN RST*



LAN REQ*

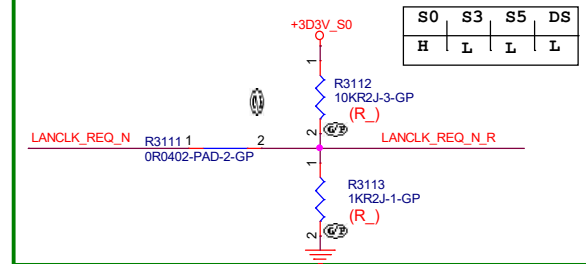


```
LINK_ACTIVITY_N==>RJ_LED0
SPEED_100_N    ==>RJ_LED1
SPEED_1000_N   ==>RJ_LED2
```



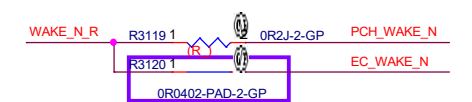
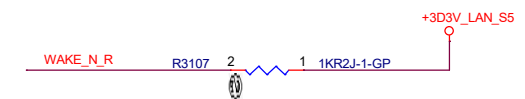
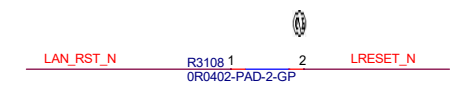
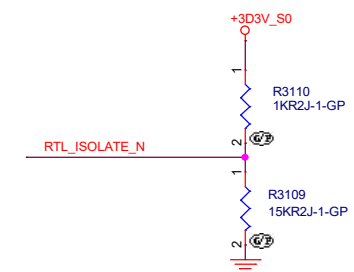
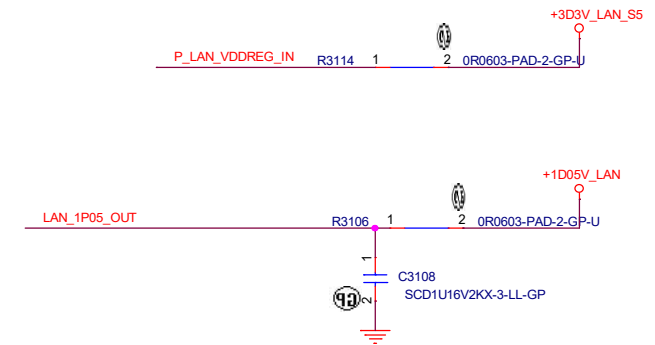
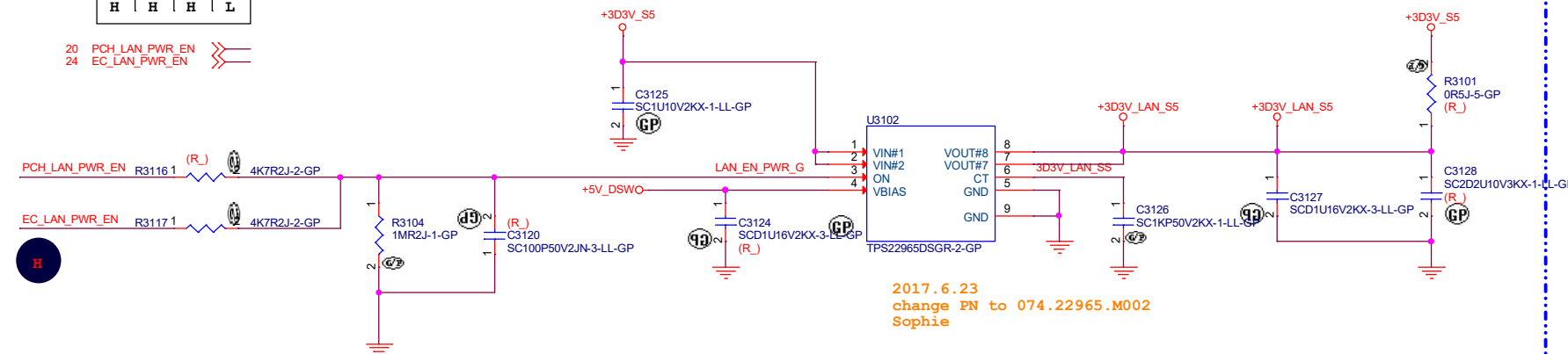
LAN CLKREQ# (LAN power saving mode)

| | | | |
|----|----|----|----|
| S0 | S3 | S5 | DS |
| H | L | L | L |



V 3P3 LAN

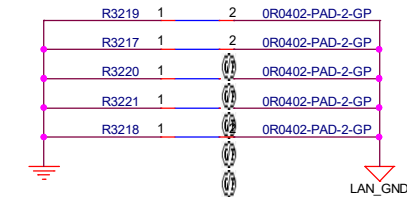
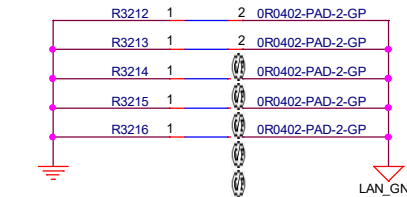
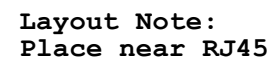
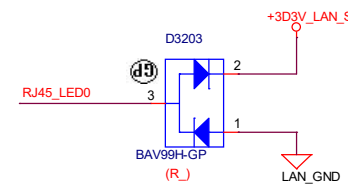
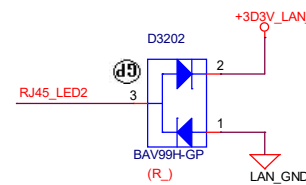
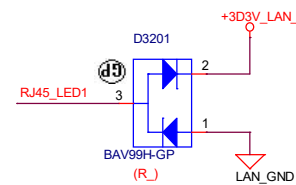
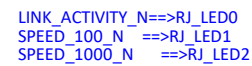
| | | | |
|----|----|----|----|
| S0 | S3 | S5 | DS |
| H | H | H | L |



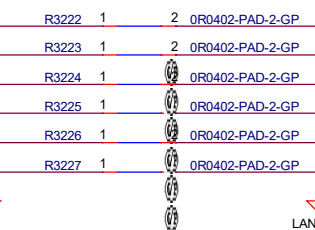
2018.3.29 SVT
change to short pad
Sophie

Left LED

Right LED

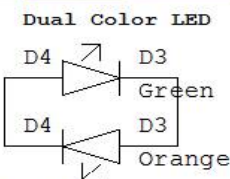


Layout Note:
Place around RJ45

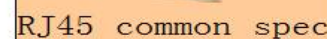


(1) LAN LED Status

| | |
|-----------|-----------|
| always on | always on |
| always on | always on |
| always on | always on |
| blinking | blinking |



(2) need to follow "RJ45 common spec"

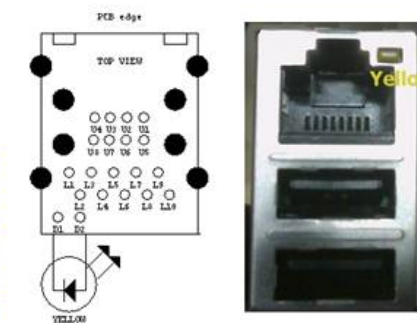


(1) LAN LED Status

(2) Yellow: Domin Wavelength (λ_p) 582-593nm, Luminous Intensity (Iv) 12-50mcd.

☐ always on

☐ blinking

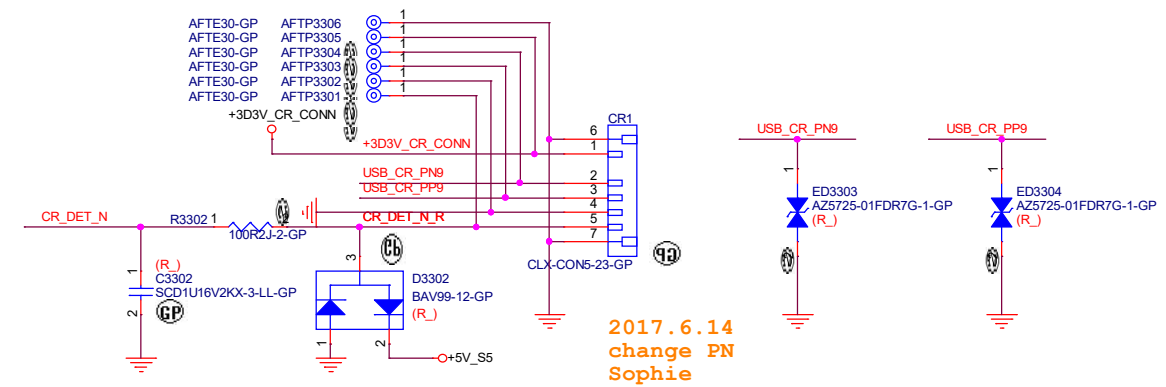
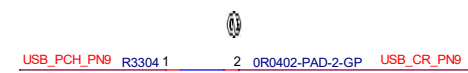
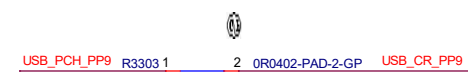
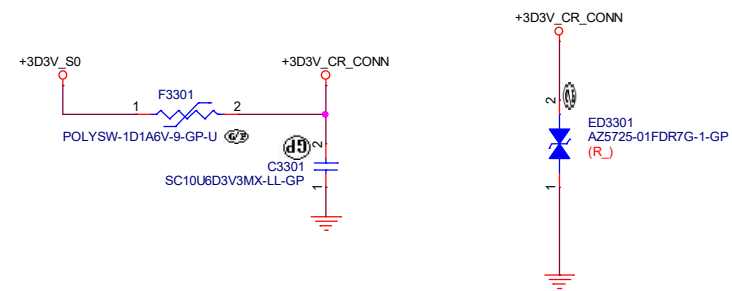


Card Reader

Card Reader

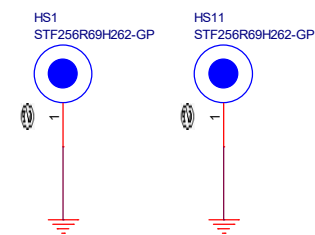
Card Reader

16 USB_PCH_PN9
16 USB_PCH_PP9
15 CR_DET_N



2017.6.14
change PN
Sophie

2017.6.16
add HS1,HS11
Sophie



USB2.0

16 USB_PCH_PN2
16 USB_PCH_PP2

USB3.0

19 USB30_TX_PCH_P2
19 USB30_TX_PCH_N2
19 USB30_RX_PCH_P2
19 USB30_RX_PCH_N2

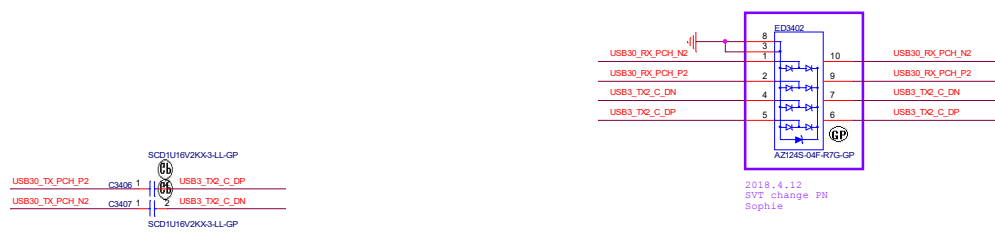
OTHERS (From ECIO)

24 USB2_OC1
24 USB_CHARGE_FAULT_N
24 ECIO_CHARGE_EN

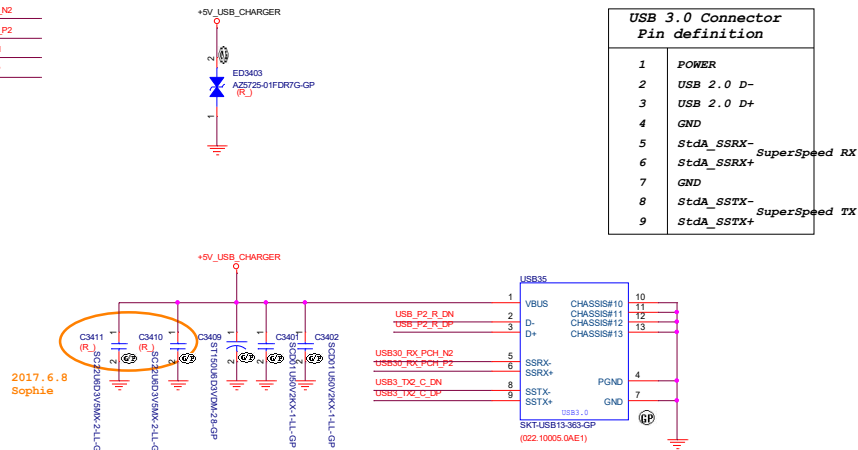
CHARGER CTRL (From ECIO)

24 ECO_ILIM_SEL
24 ECO_CHARGE_CTL1
24 ECO_CHARGE_CTL2
24 ECO_CHARGE_CTL3

For EMI TEST



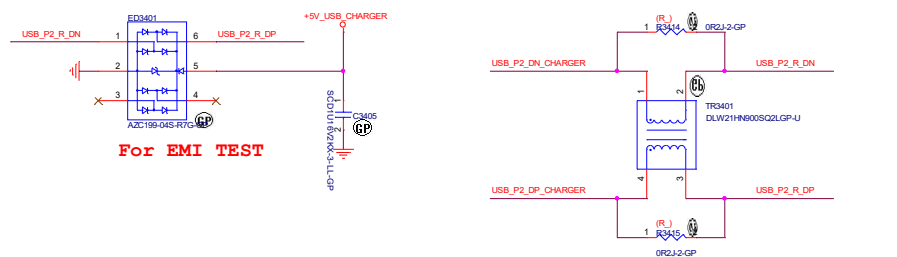
SIDE USB3.0 CONNECTOR



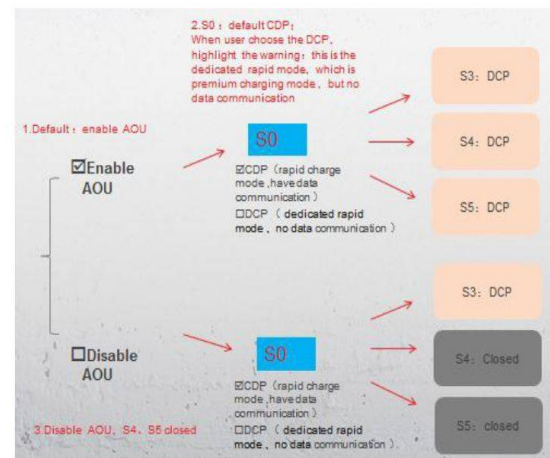
USB 3.0 Connector Pin definition

| | |
|---|--------------------------|
| 1 | POWER |
| 2 | USB 2.0 D- |
| 3 | USB 2.0 D+ |
| 4 | GND |
| 5 | StdA_SSRX- SuperSpeed RX |
| 6 | StdA_SSRX+ SuperSpeed RX |
| 7 | GND |
| 8 | StdA_SSTX- SuperSpeed TX |
| 9 | StdA_SSTX+ SuperSpeed TX |

For EMI TEST



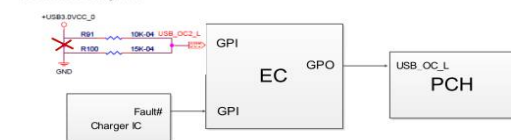
1.2 DPM AP Function Control Introduce



6.3 Fault# signal application

Charger IC Fault# would trigger during over-temperature and current limit conditions and the charger IC would reset SMBUS (reset voltage and current) when Portable devices contact with Charger. So it would be erroneous triggered under current-limit and Charger IC discharger conditions.

6.3.1Blok Diagram



6.3.2 EC control

EC use traditional OC# and Charger IC Fault# to operation program to indicate short condition.
S0: Detect that if IC fault# signal is triggered, EC assert OC# to PCH.
S3: Detect that traditional OC# and Charger IC fault# are both triggered, EC assert OC# to PCH.

Note:

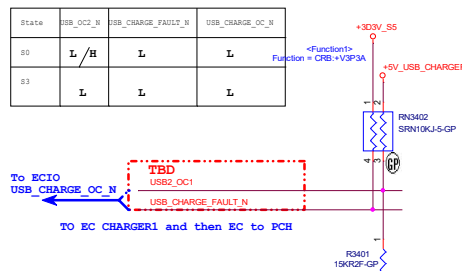
- 1) All shaded boxes are device charging modes
- 2) See below table for CTL settings corresponding to flow line conditions

| | Device Control Pins | | | |
|---------------------|---------------------|------|------|----------|
| Flow Line Condition | CTL1 | CTL2 | CTL3 | ILIM_SEL |
| DCH | 0 | 0 | 0 | X |
| CDP | 1 | 1 | 1 | 1 |
| SDP2 | 1 | 1 | 1 | 0 |
| SDP1 | 1 | 1 | 0 | X |
| | 0 | 1 | 0 | X |
| DCP_SHORT | 1 | 0 | 0 | X |
| DCP_DIVIDER | 1 | 0 | 1 | X |
| DCP_Auto | 0 | 1 | 1 | X |
| | 0 | 0 | 1 | X |

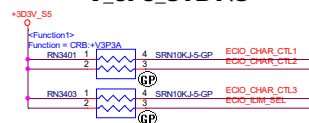
Default status:

| ECIO_CHAR_CTL1 | ECIO_CHAR_CTL2 | ECIO_CHAR_EN | Mode | State |
|----------------|----------------|--------------|--|------------------------------|
| 1 | 1 | 1 | CDP | S0 |
| 0 | 1 | 1 | DCP with HID auto detect USB data pass through | S3 |
| 0 | 0 | 1 | DCP | S4/S5 |
| 0 | 0 | 0 | Shut down | EN DSW and DIS CHAR on S4/S5 |

ILIM_L0 51Kohm:0.9A
ILIM_HI 33Kohm:1.5A
Lenovo HW Spec change
ILIM_HI:2.1A To 1.5A



V_3P3_STBY/G



MODE SELECT by ECIO

| | | | |
|----------------|---------|-----------------|-----------------|
| ECIO_CHAR_EN | R3405 1 | 0R0402-PAD-2-GP | CHARGE_EN1 |
| ECIO_CHAR_CTL1 | R3406 1 | 0R0402-PAD-2-GP | USB_CHARGE_CTL1 |
| ECIO_CHAR_CTL2 | R3407 1 | 0R0402-PAD-2-GP | USB_CHARGE_CTL2 |
| ECIO_CHAR_CTL3 | R3408 1 | 0R0402-PAD-2-GP | USB_CHARGE_CTL3 |
| ECIO_ILIM_SEL | R3409 1 | 0R0402-PAD-2-GP | ILIM_SEL |

Control pin Truth Table Setting

| Mode | CTL1 | CTL2 | CTL3 | ILIM_SEL |
|-------------|------|------|------|----------|
| SDP (S3) | 1 | 1 | 1 | 0 |
| CDP (S0) | 1 | 1 | 1 | 1 |
| DCP (S4/S5) | 0 | 0 | 1 | 1 |

Reserved

USB2.0 * 4 ==>

16 USB_PCH_PP4
16 USB_PCH_PN4

8,20,24,37,40,65 SLP_S4_N

USB3.0 * 4 ==>

19 USB30_TX_PCH_N4
19 USB30_TX_PCH_P4
19 USB30_RX_PCH_P4
19 USB30_RX_PCH_N4

19 USB30_TX_PCH_P3
19 USB30_TX_PCH_N3
19 USB30_RX_PCH_P3
19 USB30_RX_PCH_N3

To PCH USB OC pin

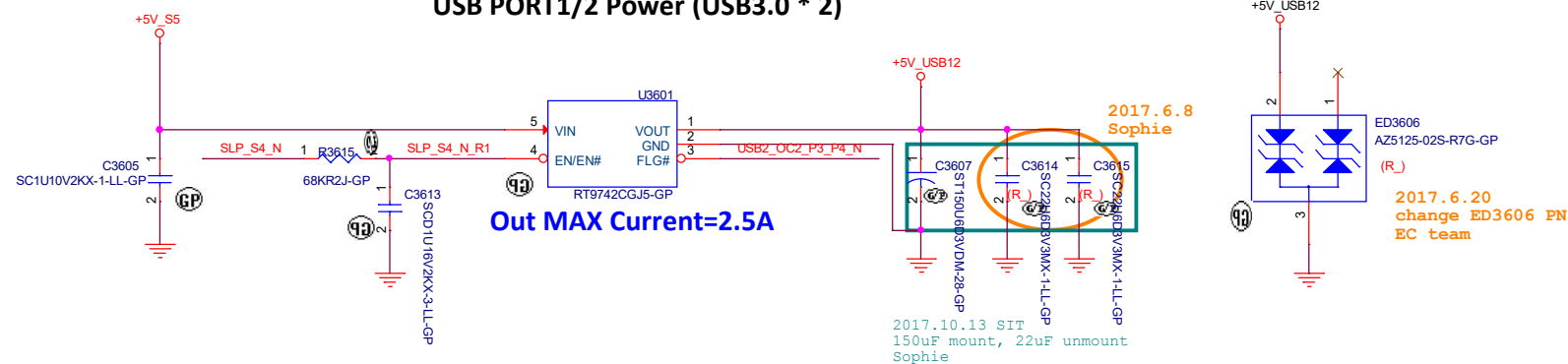
16 USB2_OC2_P3_P4_N

USB3.0 DEBUG

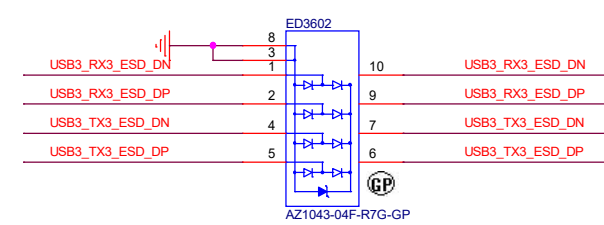
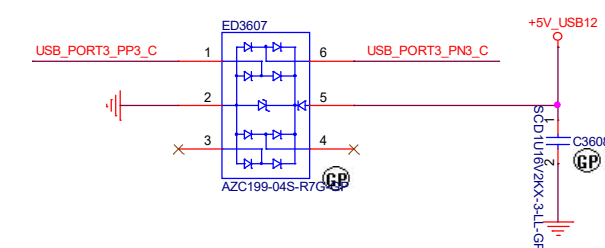
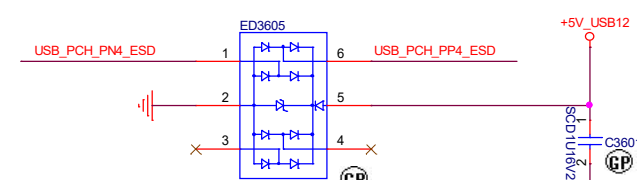
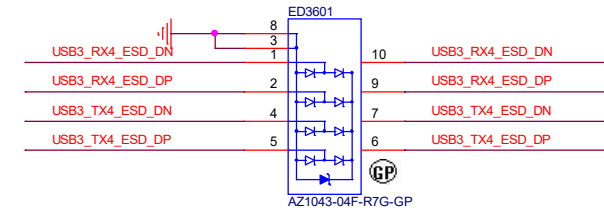
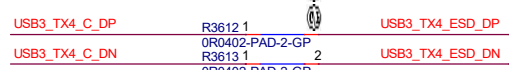
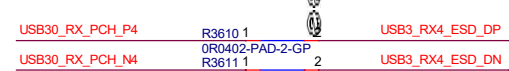
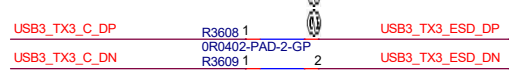
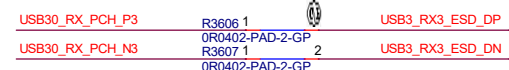
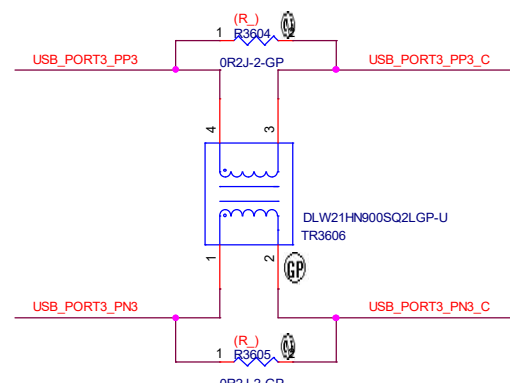
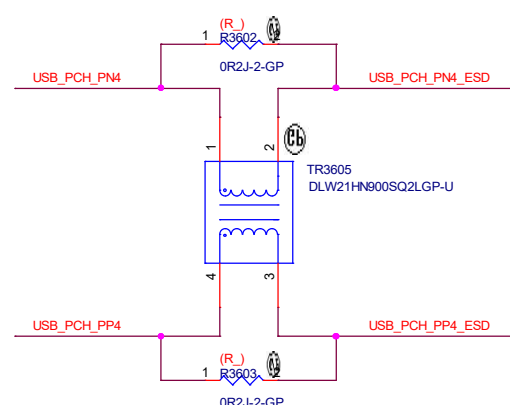
24 UART_P80_EN

24 USB_PORT3_PN3
24 USB_PORT3_PP3

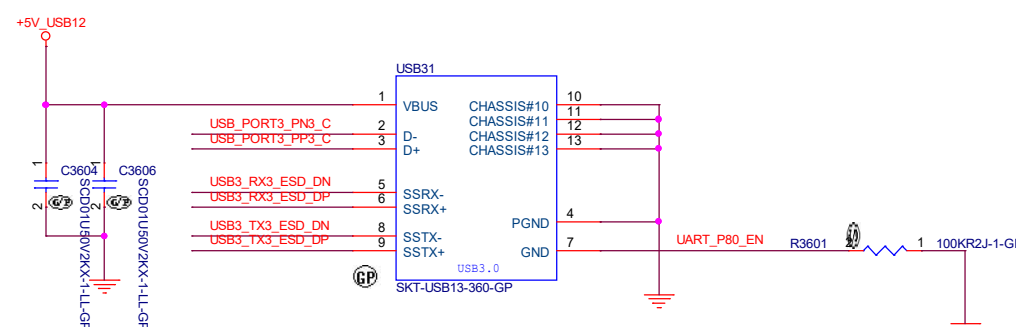
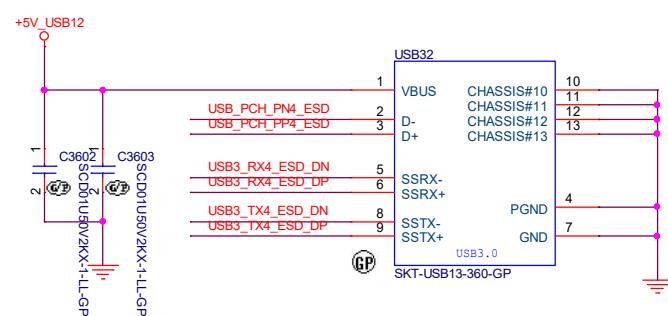
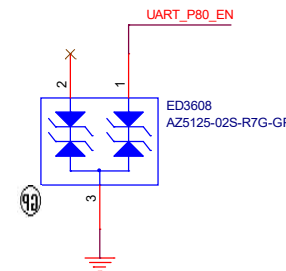
USB PORT1/2 Power (USB3.0 * 2)



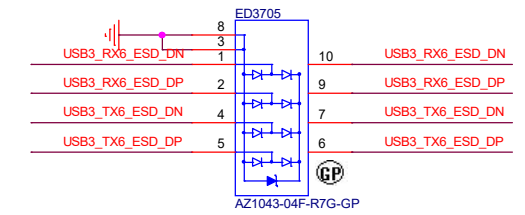
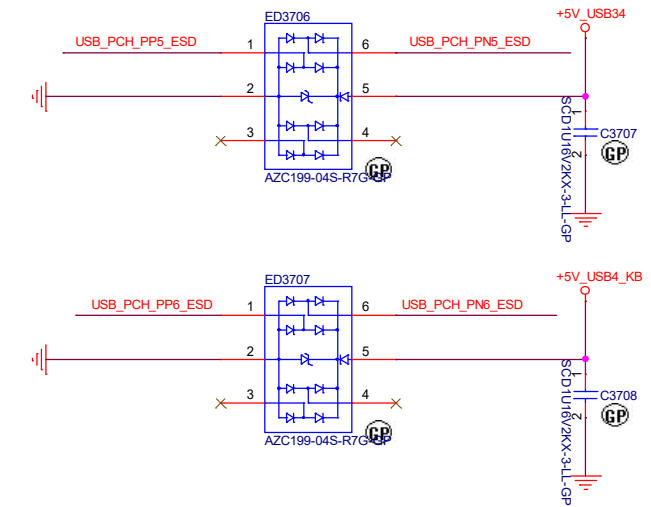
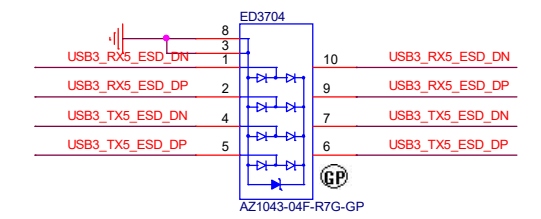
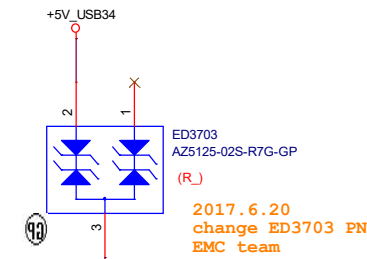
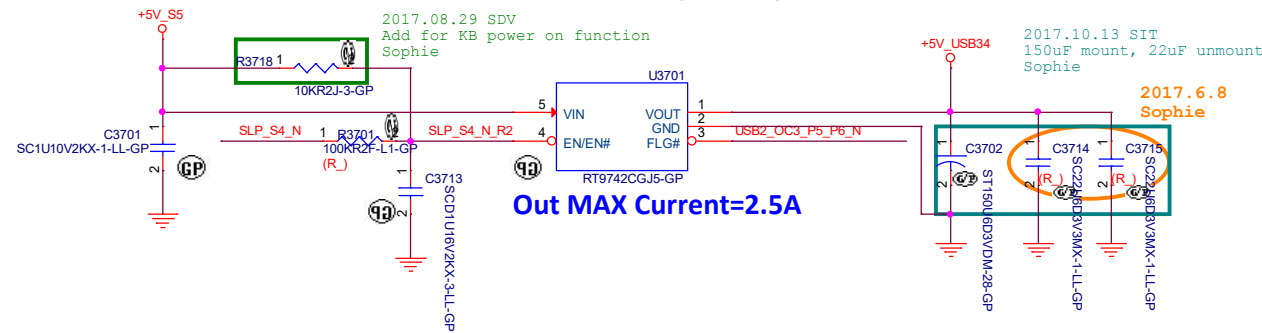
Coupling caps



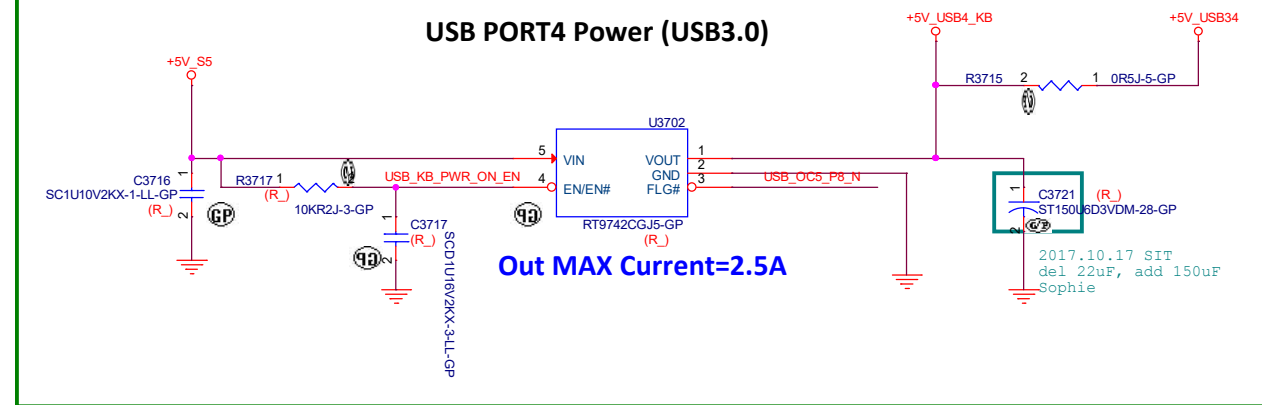
2017.6.20
change ED3608 PN
EMC team



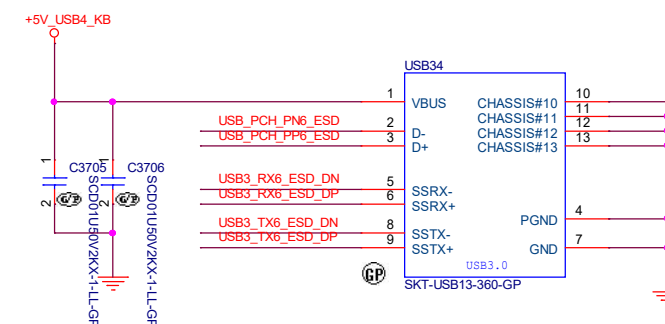
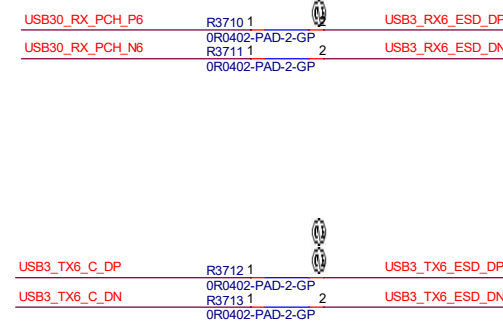
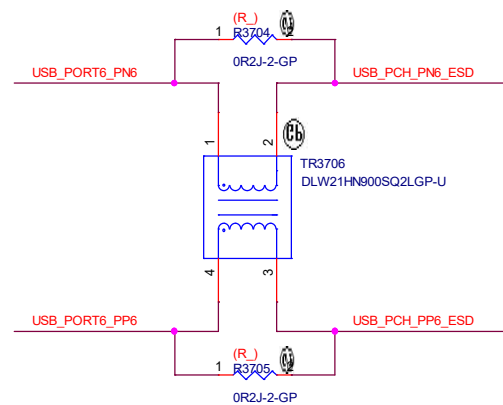
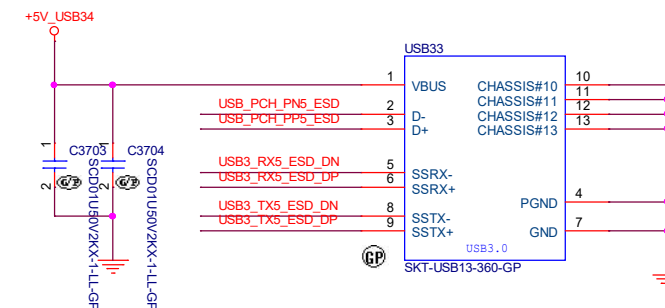
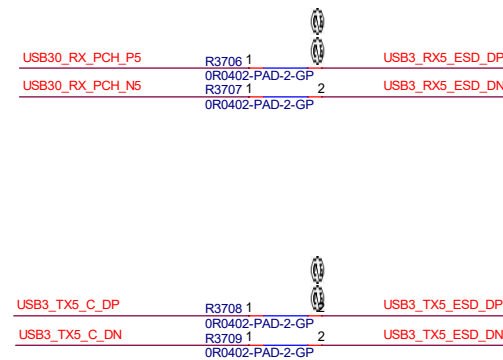
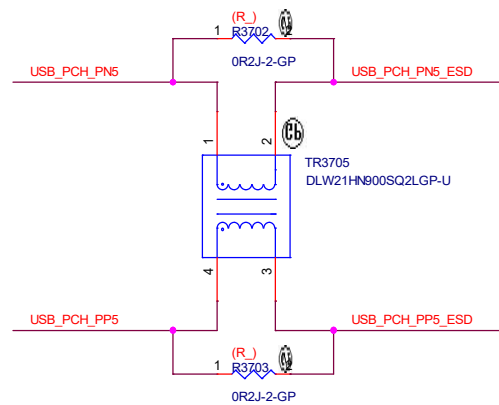
USB PORT3 Power (USB3.0)



USB PORT4 Power (USB3.0)



2017.08.29 SDV
Add for KB power on function
Sophie



```

16  USB_PCH_PN1  << >>
16  USB_PCH_PP1  << >>

```

16 USB2_OC0_P1_N <<—

16 USBC_VCONN_OC_N <<—

USB3.0 * 4 ==>

PCH end

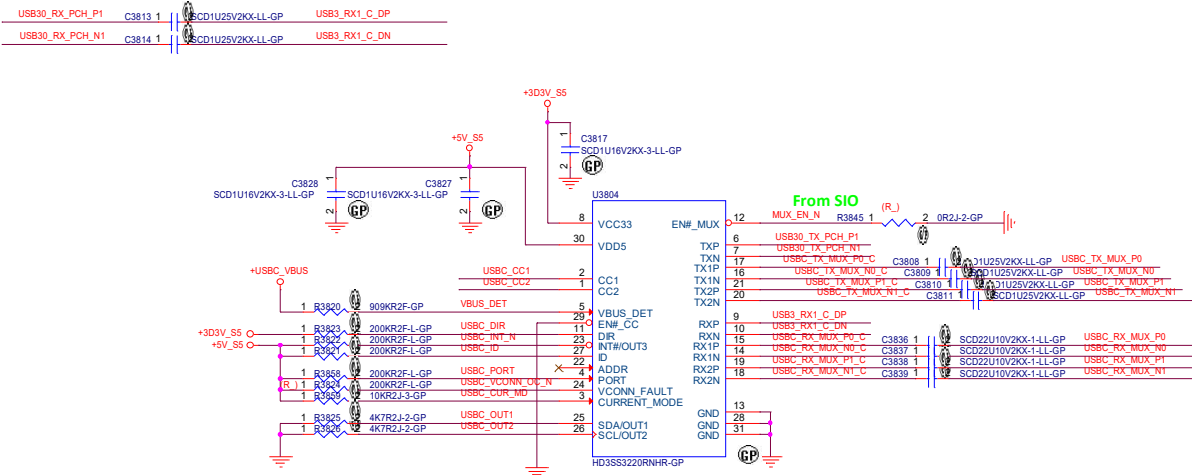
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19  USB30_TX_PCH_N1
19  USB30_TX_PCH_P1
19  USB30_RX_PCH_P1
19  USB30_RX_PCH_N1

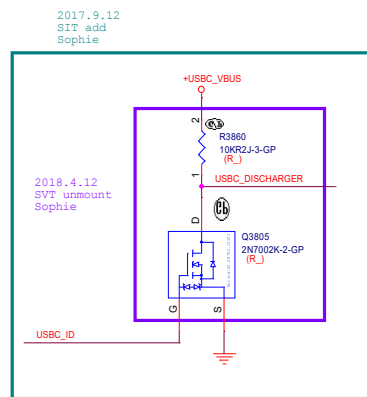
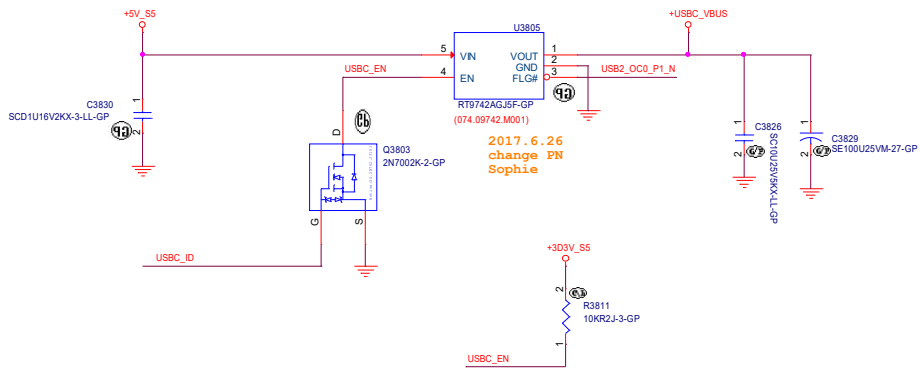
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24 MUX_EN_N

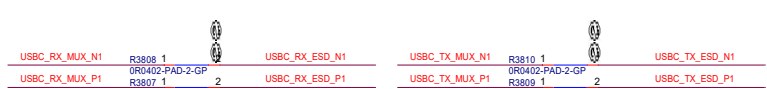
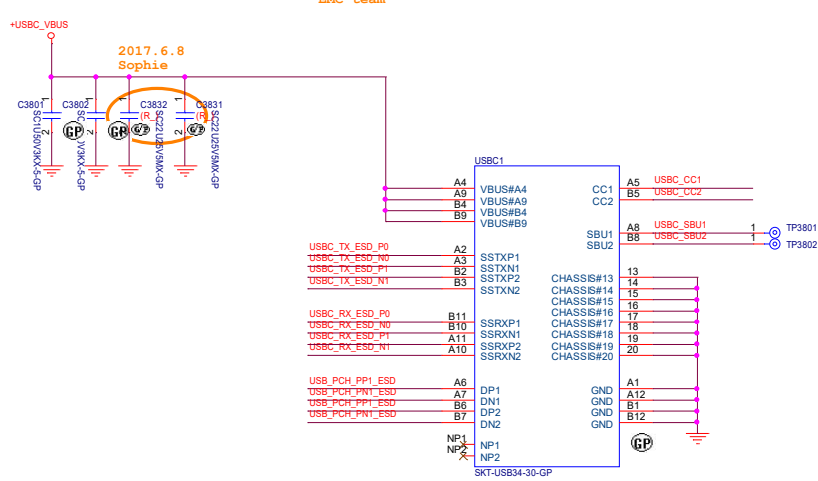
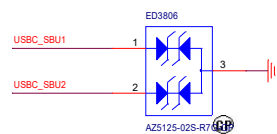
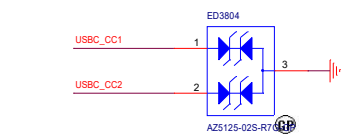
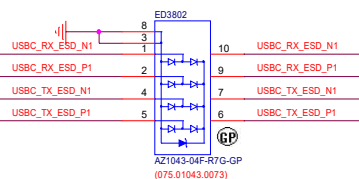
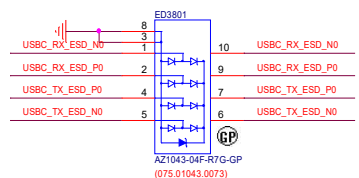
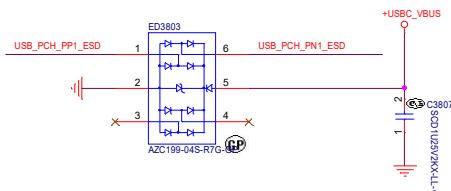
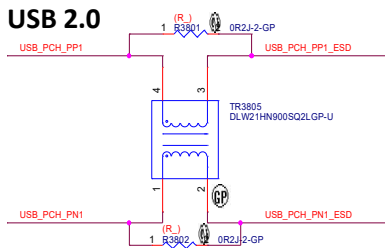
4 USBC_DIR <<—



PORT - DFP mode(H)
DIR - Pull 200K to High
Current mode - 3A (Pull 10K to High)
INT_N - Pull 200K to High
OUT1 - 3A setting to GND
OUT2 - High current mode detect to GND



USB 2.0



D

C

B

A

5

4

3

2

1


D

C

B

A

Reserved

| | | | |
|---|---------------------------|---|-----------|
|  | | Wistron Incorporated 12F, 88, Hsin Tai Wu Rd Hsichih, Taipei | |
| Title 039_USB30_# (R) | | | |
| Size A | Document Number LM820Z | | Rev SA |
| Date: | Thursday, April 19, 2018 | Sheet | 39 of 107 |

5

4

3

2

1

Mask circuit for PSU ON and normal power

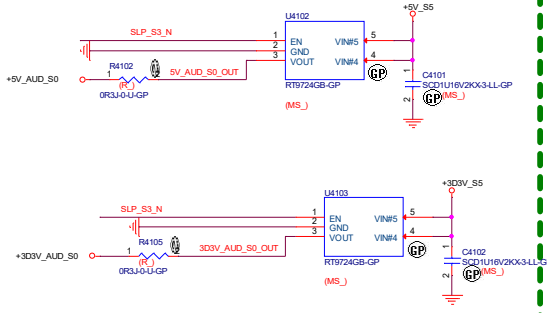
NOR, AND GATE

Table 4. Function table[1]

| Input | | Output | |
|-------|---|--------|---|
| C | B | A | Y |
| L | L | L | L |
| L | L | H | L |
| L | H | L | H |
| L | H | H | H |
| H | L | L | L |
| H | L | H | H |
| H | H | L | L |
| H | H | H | H |

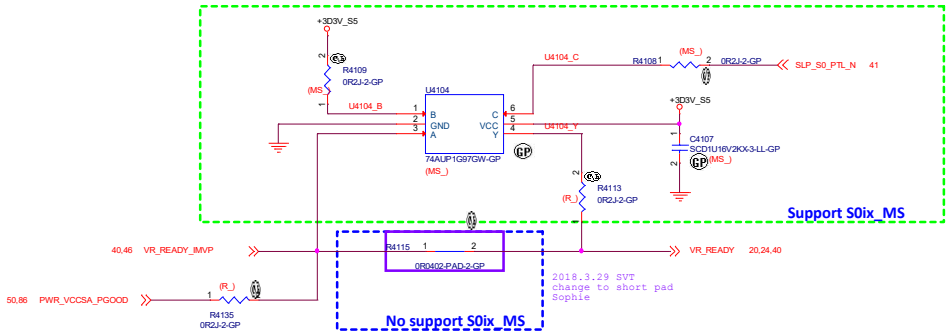
[1] H = HIGH voltage level;
L = LOW voltage level.

For Audio



Support S0ix_MS

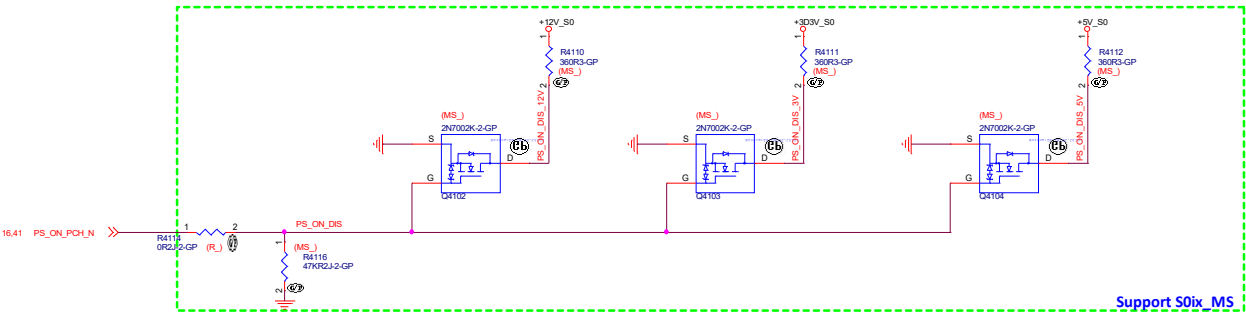
Mask circuit for VR_READY



Support S0ix_MS

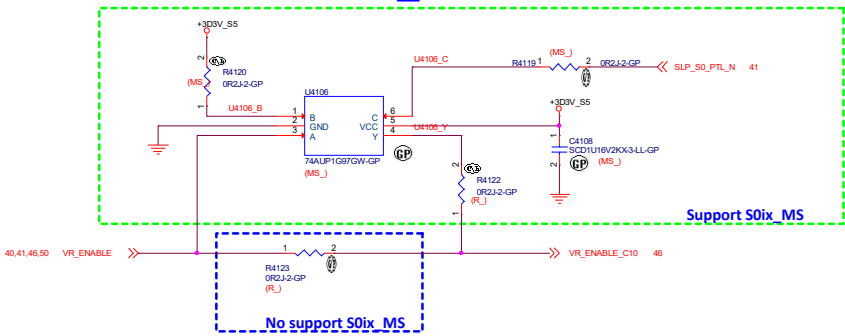
No support S0ix_MS

Discharge circuit



Support S0ix_MS

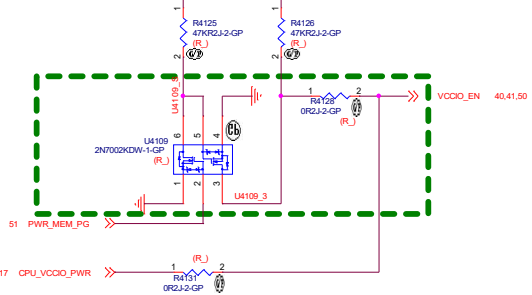
Mask circuit for VR_ENABLE



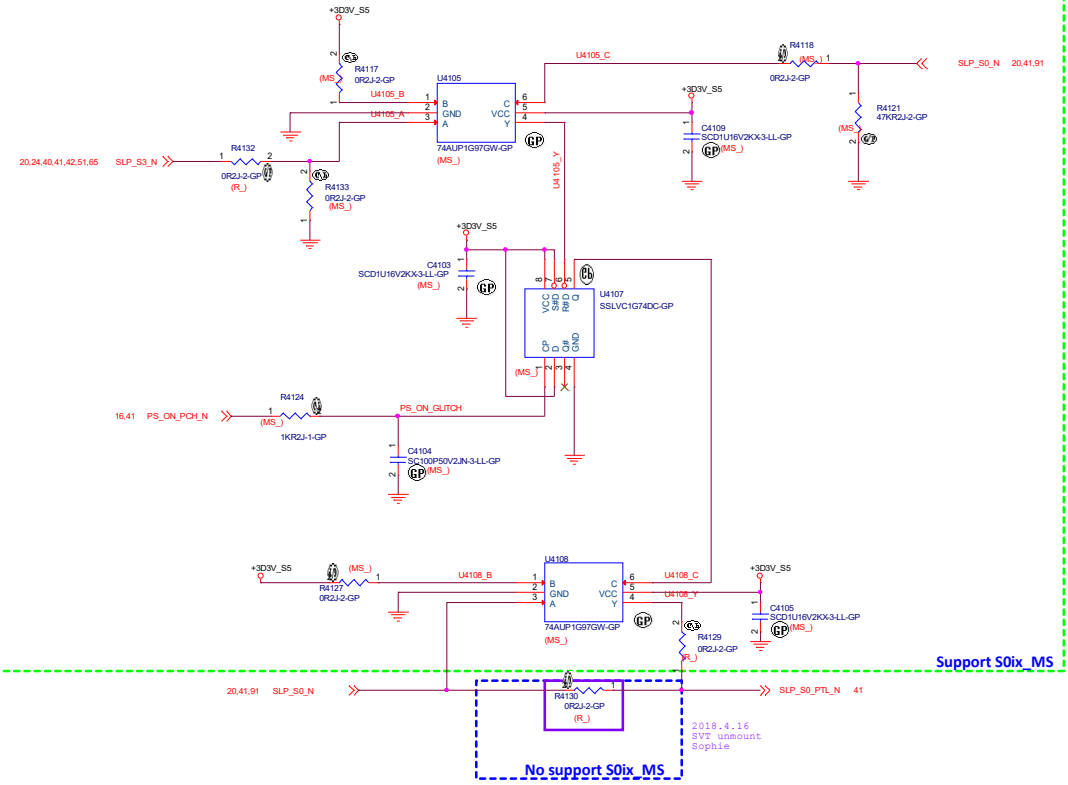
Support S0ix_MS

No support S0ix_MS

VCCIO control circuit

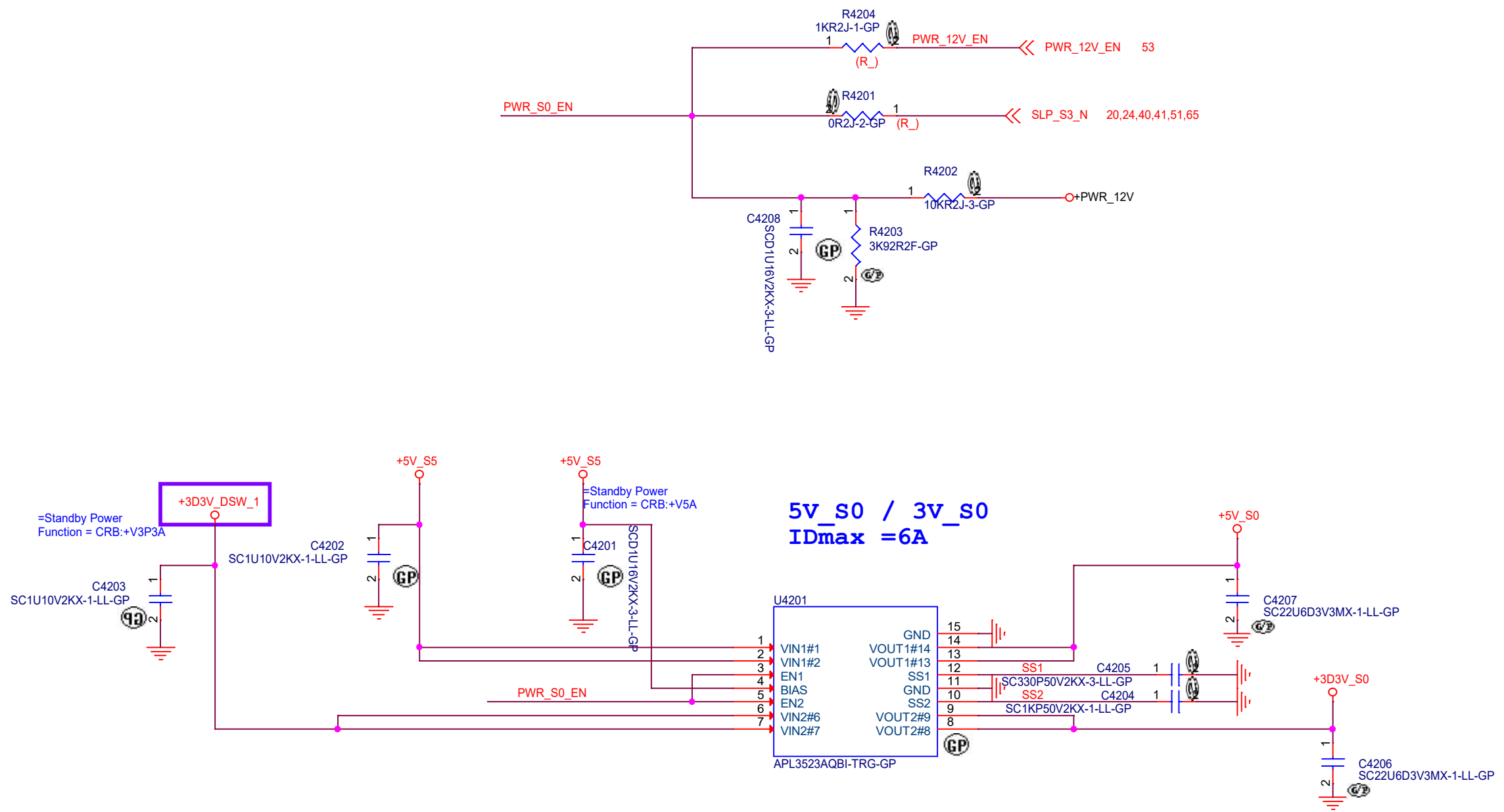


Glitch free circuit



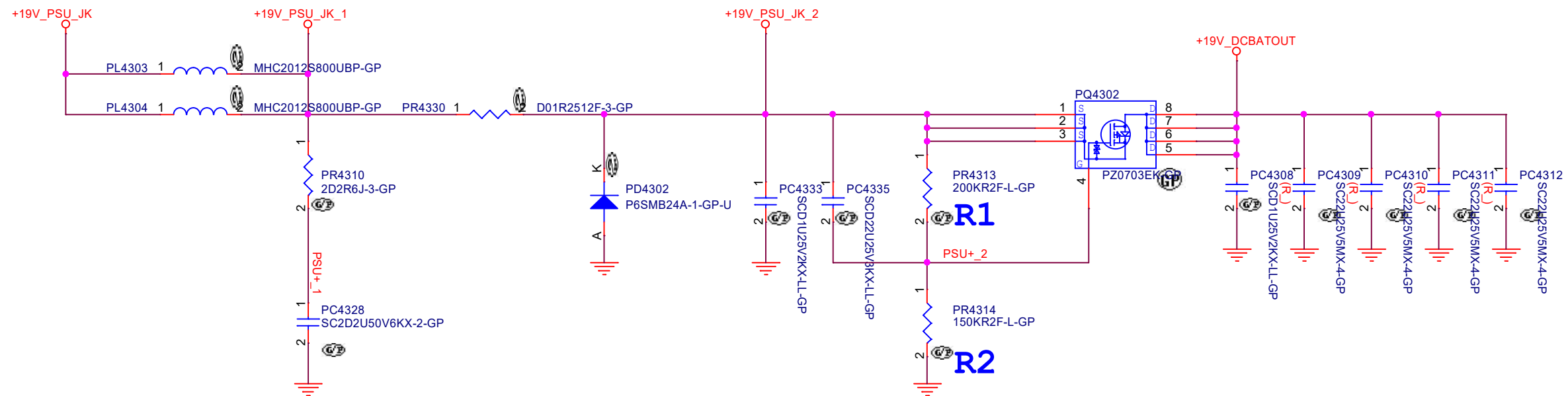
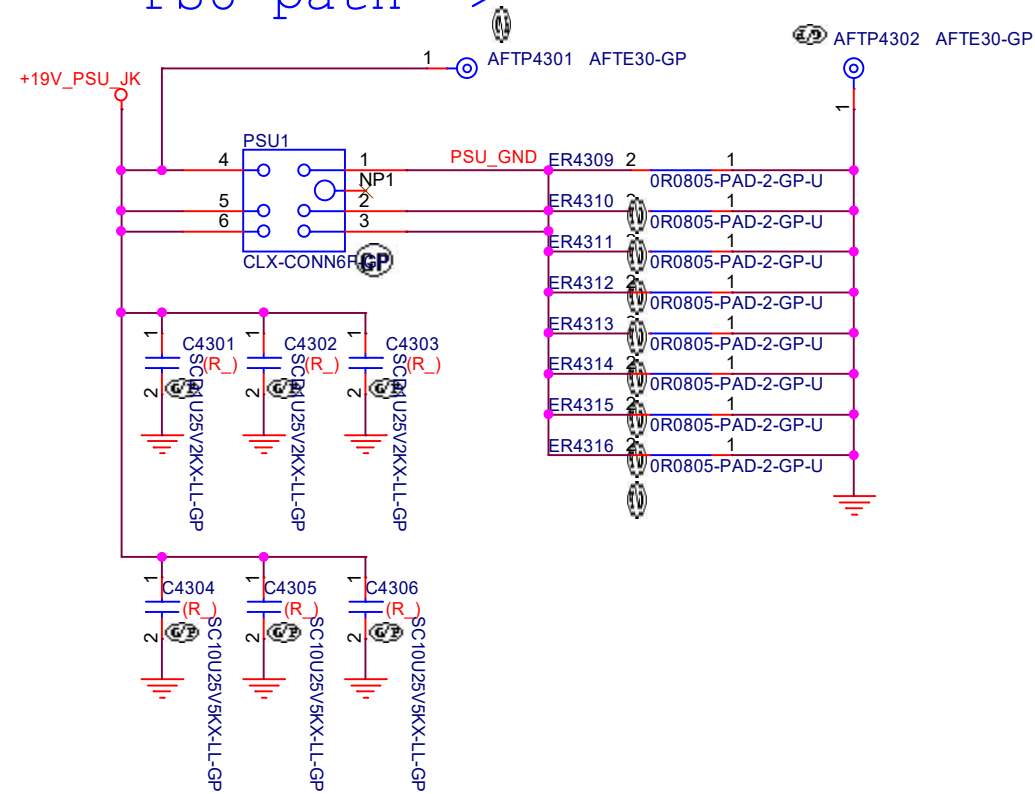
Support S0ix_MS

No support S0ix_MS



5V_S0 / 3V_S0
IDmax =6A

PSU path==>



Snubber R use >2ohm 1206 or 1210 size .
Snubber C use 2.2uF .X5R or X7R 1206 size

Softstart <=3ms . R1=200K , R2=150K . C=0.22uF.
PQ4302 need choose PZ0703EK .

wistron

Wistron Incorporated
12F, 88, Hsin Tai Wu Rd
Hsichih, Taipei

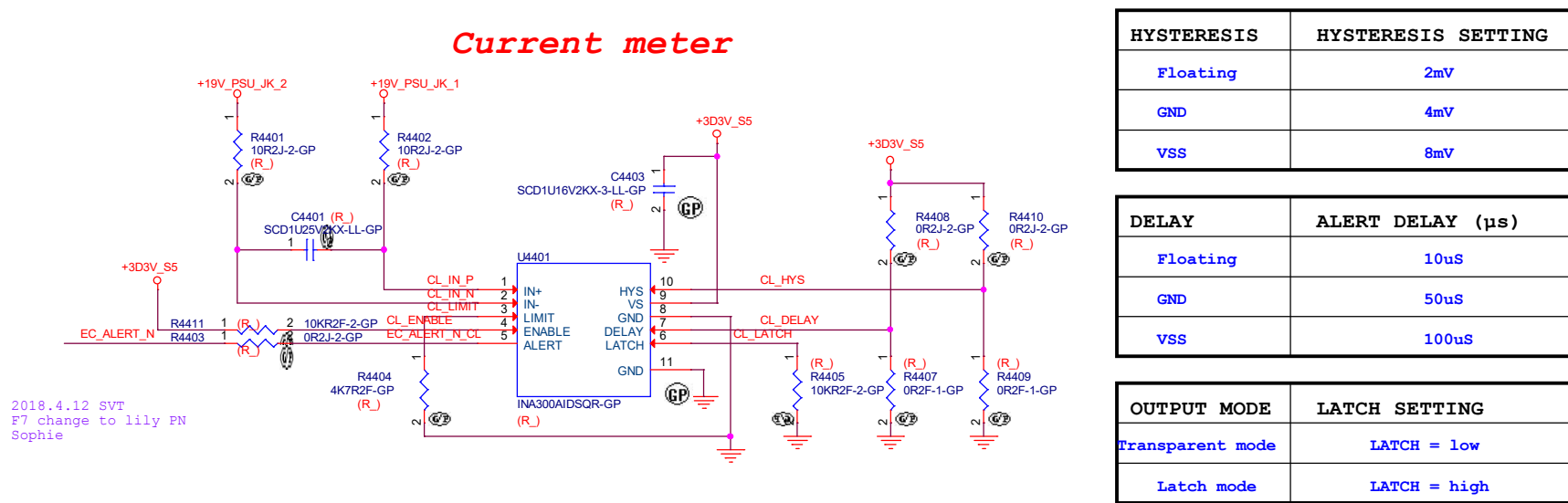
Title
043_ATX(BATT Conn)

Size Document Number
Custom LM820Z

Date: Thursday, April 19, 2018

Sheet 43 of 107

Rev
SA

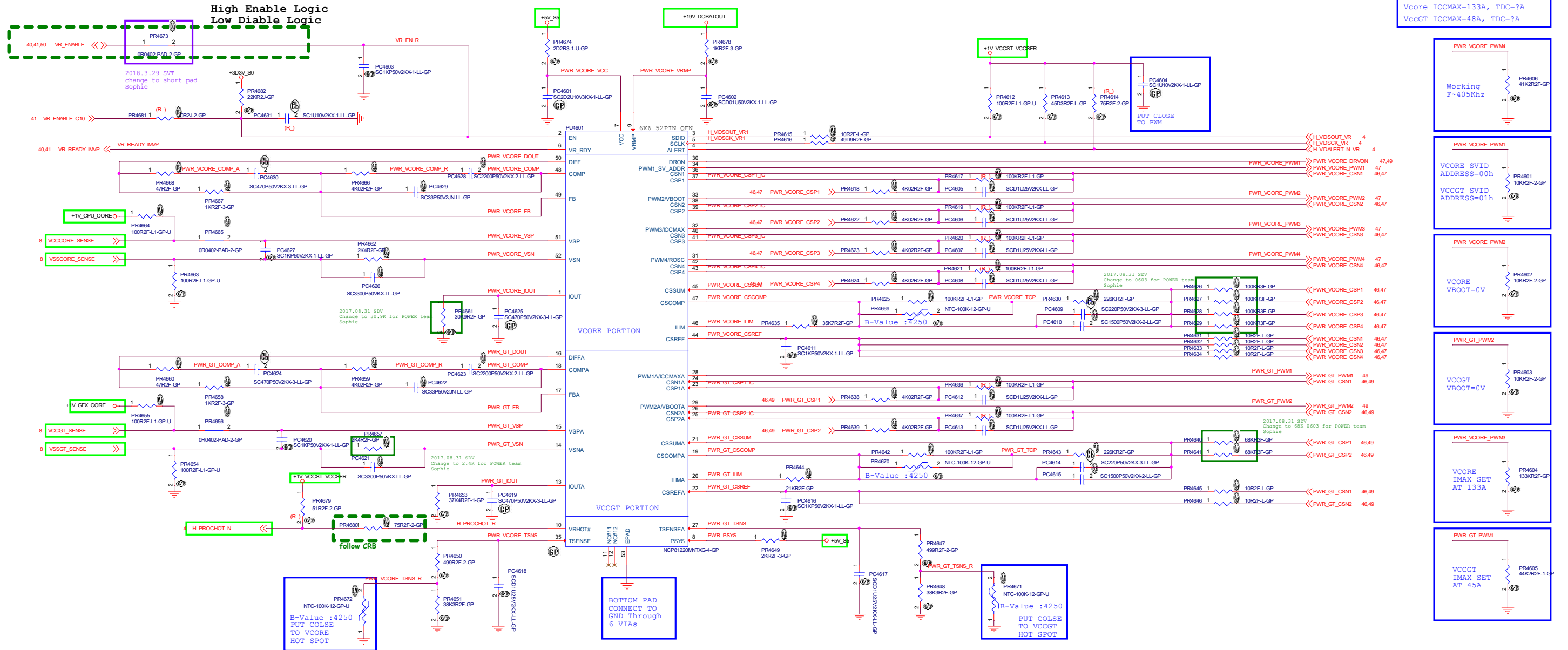


| | PARAMETER | EQUATION |
|-----------|------------------------------------|--------------------------------------|
| VTRIP | Desired current trip value | $I_{LOAD} \times R_{SENSE}$ |
| VLIMIT | Programmed threshold limit voltage | $V_{LIMIT} = V_{TRIP}$ |
| VLIMIT(1) | Threshold voltage | $(I_{LIMIT} \times R_{LIMIT}) - NAF$ |
| RLIMIT(1) | Threshold limit setting resistor | $(V_{LIMIT} + NAF) / I_{LIMIT}$ |
| RLIMIT(1) | Limit setting resistor | $(V_{LIMIT} + 500 \mu V) / 20 \mu A$ |

(1) NAF is used with the 10-μs delay setting. NAF can be omitted in the RLIMIT calculation for the 50-μs and 100-μs delay settings.



Intel Coffeelake IMVP8 POWER CKT - S-LINE 62 65W 4+2 PHASE



D

C

B

A

5

4

3

2

1


D

C

B

A

Reserved

| | | | |
|---|---------------------------|---|-----------|
|  | | Wistron Incorporated 12F, 88, Hsin Tai Wu Rd Hsichih, Taipei | |
| Title 048_CPU Core_# (R) | | | |
| Size A | Document Number LM820Z | | Rev SA |
| Date: | Thursday, April 19, 2018 | Sheet | 48 of 107 |

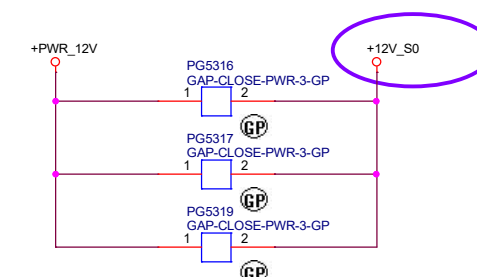
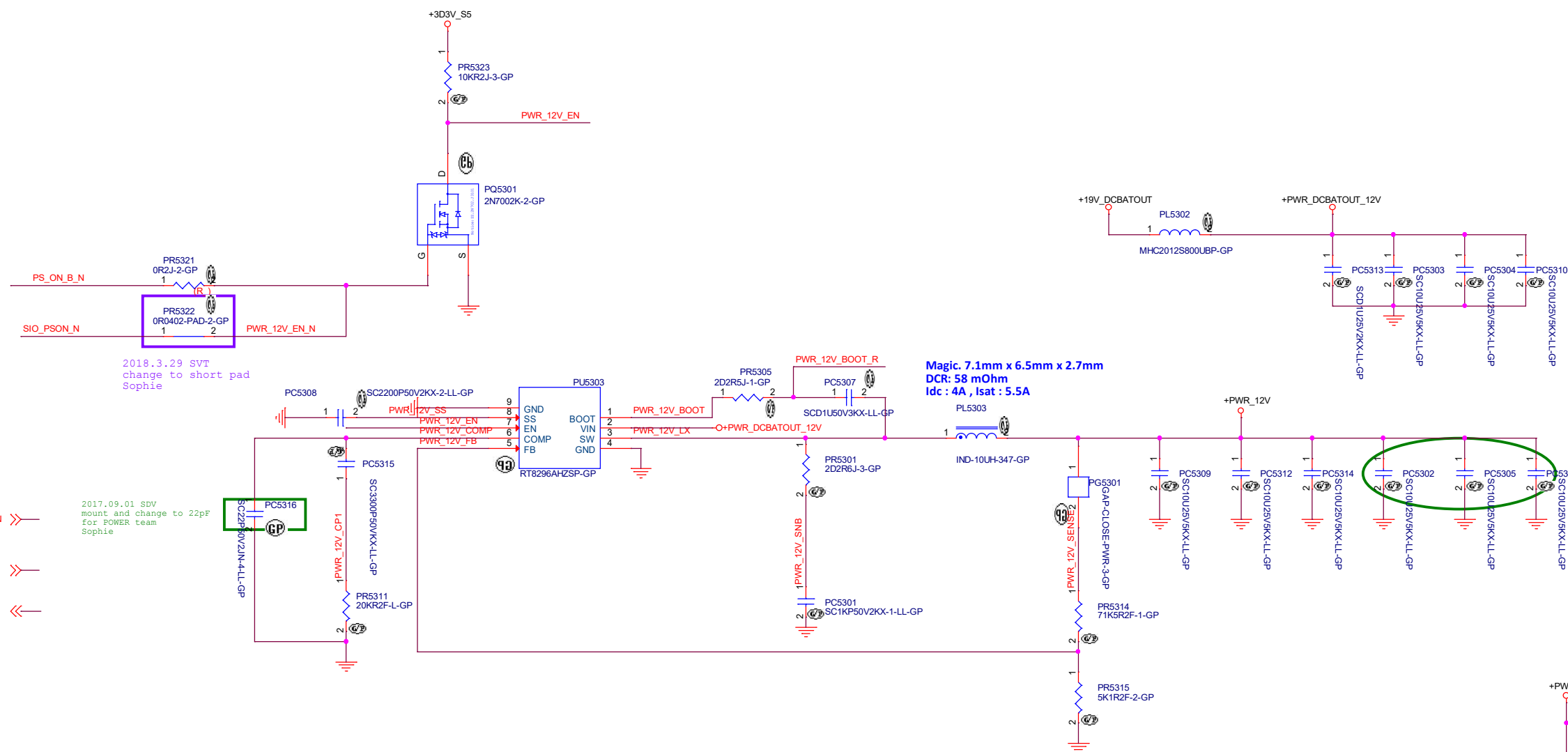
5

4

3

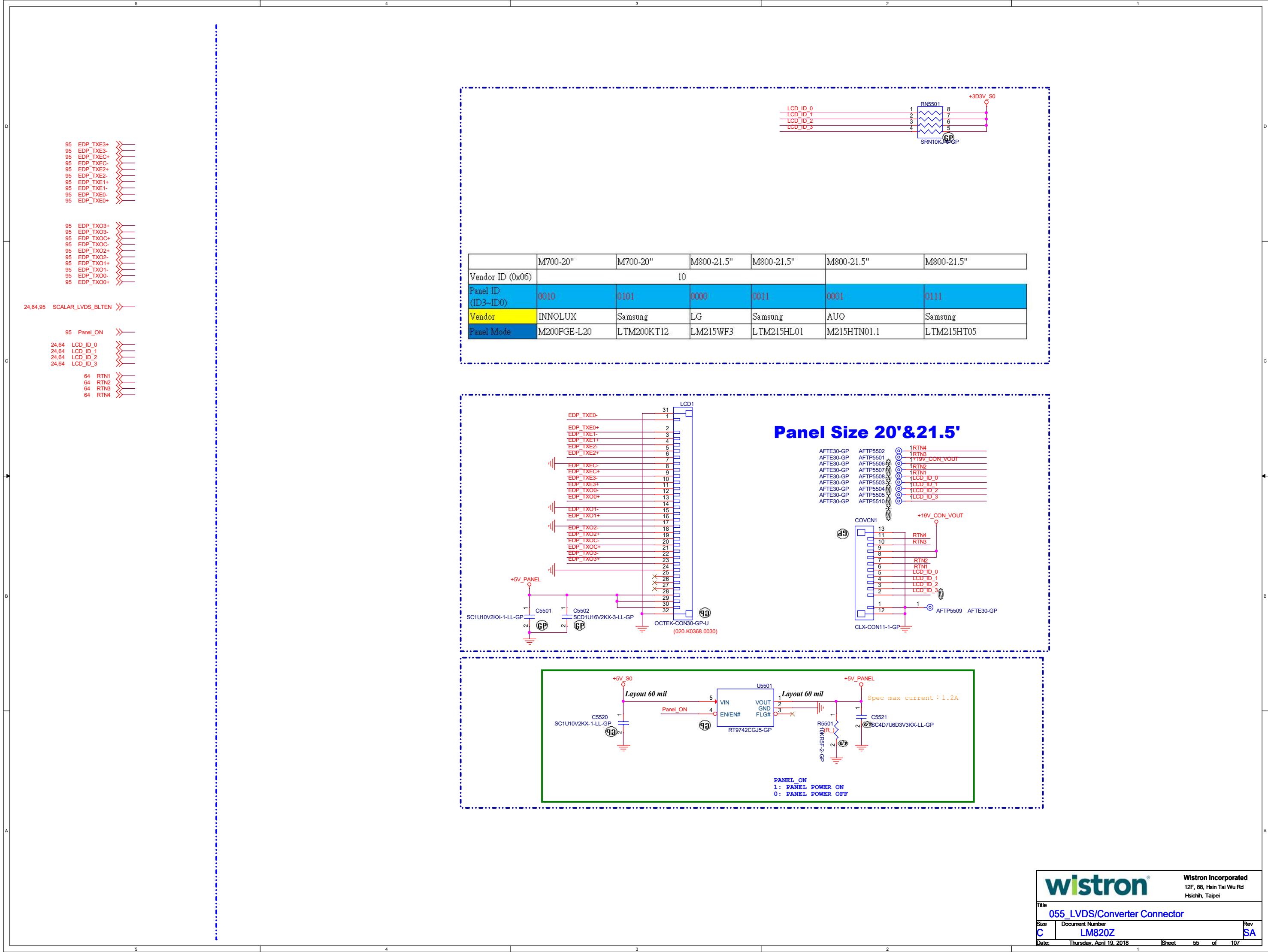
2

1



1D5V (Audio)





D

C

B

A


D

C

B

A

Reserved

| | | | |
|---|---------------------------|---|-----------|
|  | | Wistron Incorporated 12F, 88, Hsin Tai Wu Rd Hsichih, Taipei | |
| Title 056_HDMI# (R) | | | |
| Size A | Document Number LM820Z | | Rev SA |
| Date: | Thursday, April 19, 2018 | Sheet | 56 of 107 |

Switch HDMI Out Mode:
DP OUT+DP TO HDMI CABLE==>HDMI OUT

Common DP Port:
DP OUT&HDMI OUT

2017.6.13
Sophie

2017.08.21 SDV
Change DP power solution
Sophie

2016.05.18
EMC team
requirement

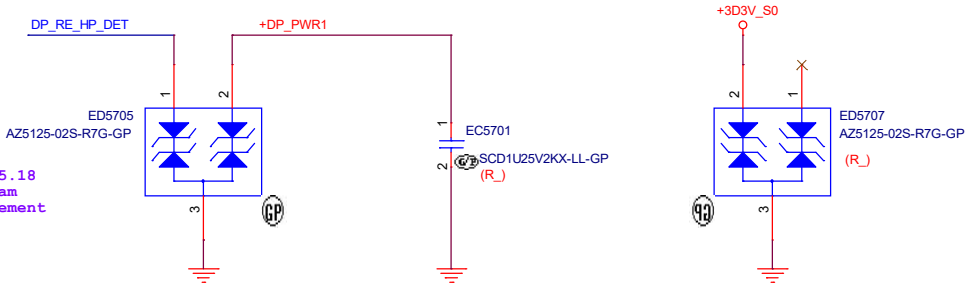
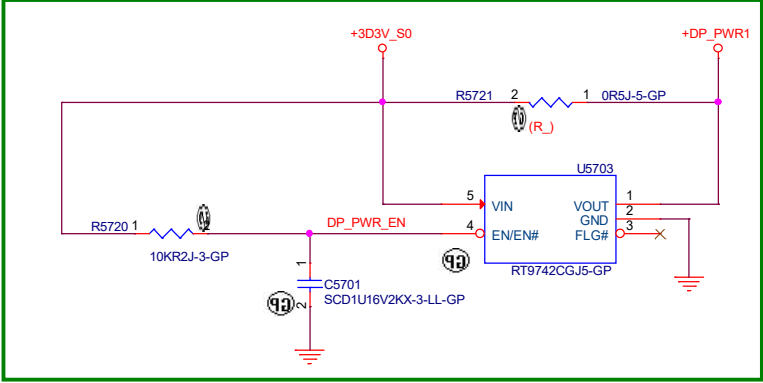
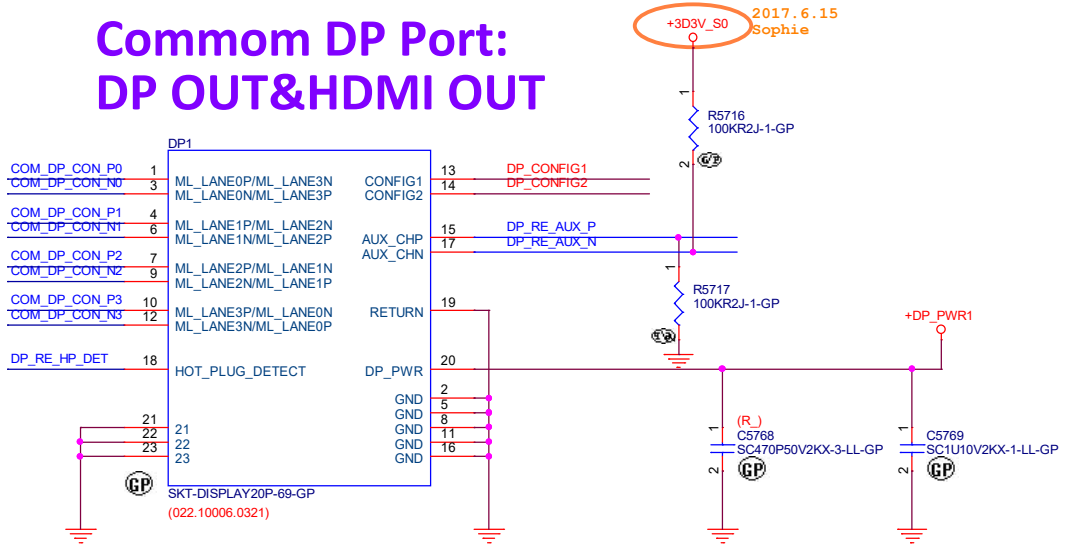
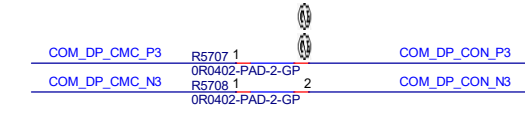
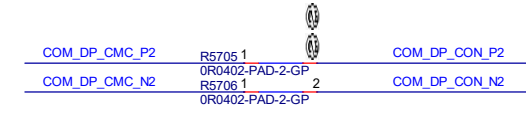
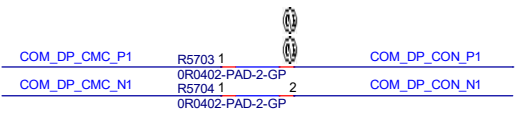
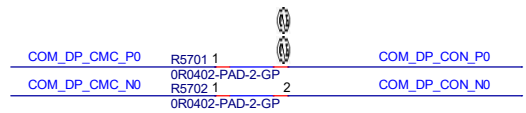
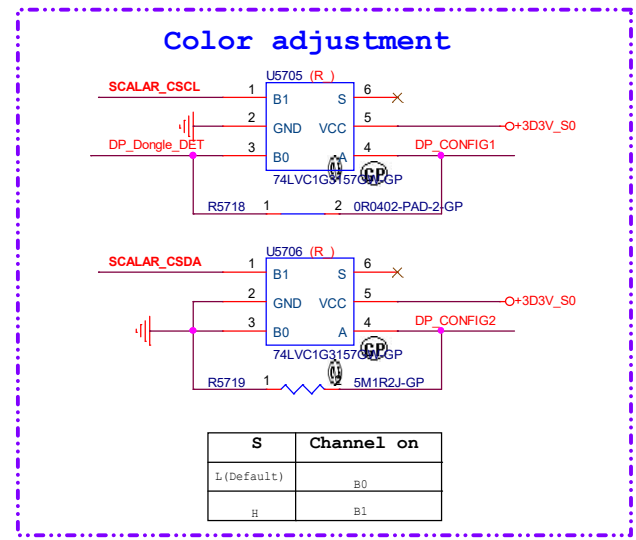
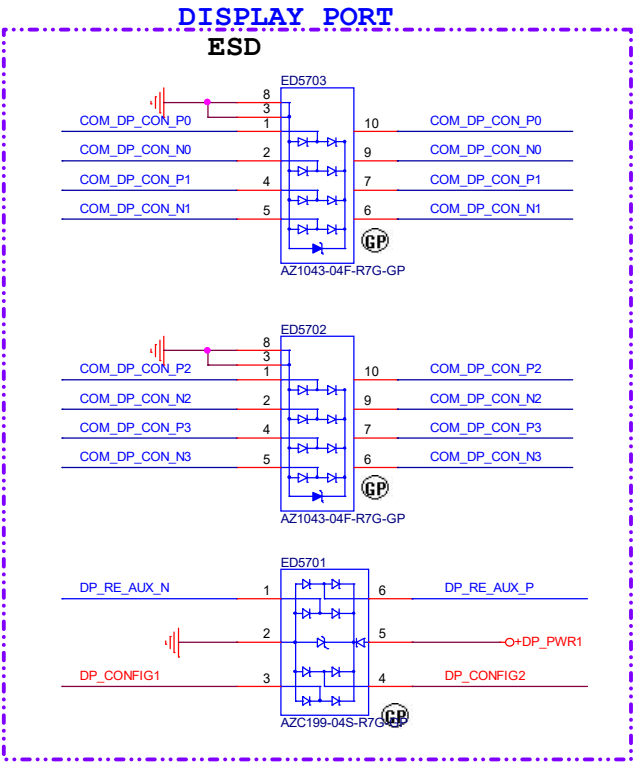
DP in for color temperature

95 SCALAR_CSCL
95 SCALAR_CSDA

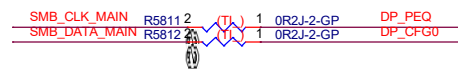
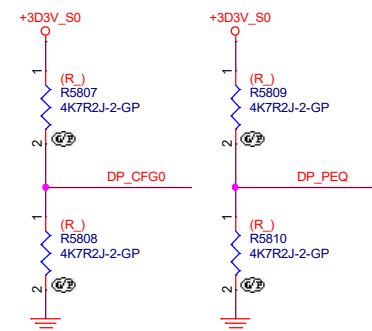
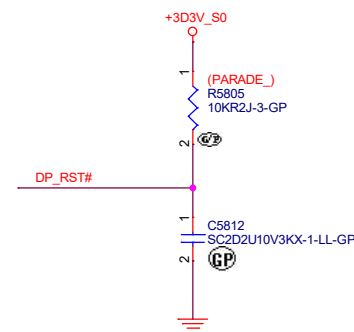
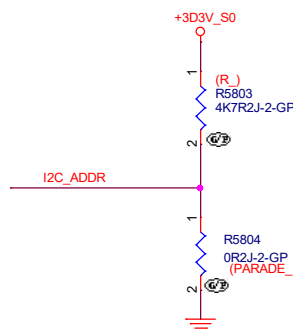
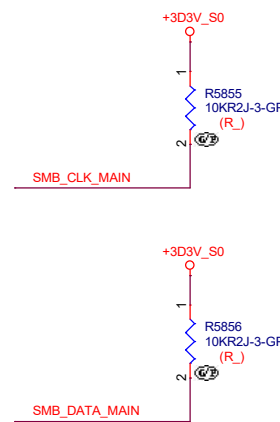
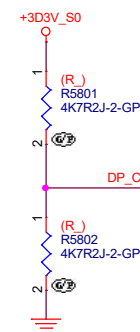
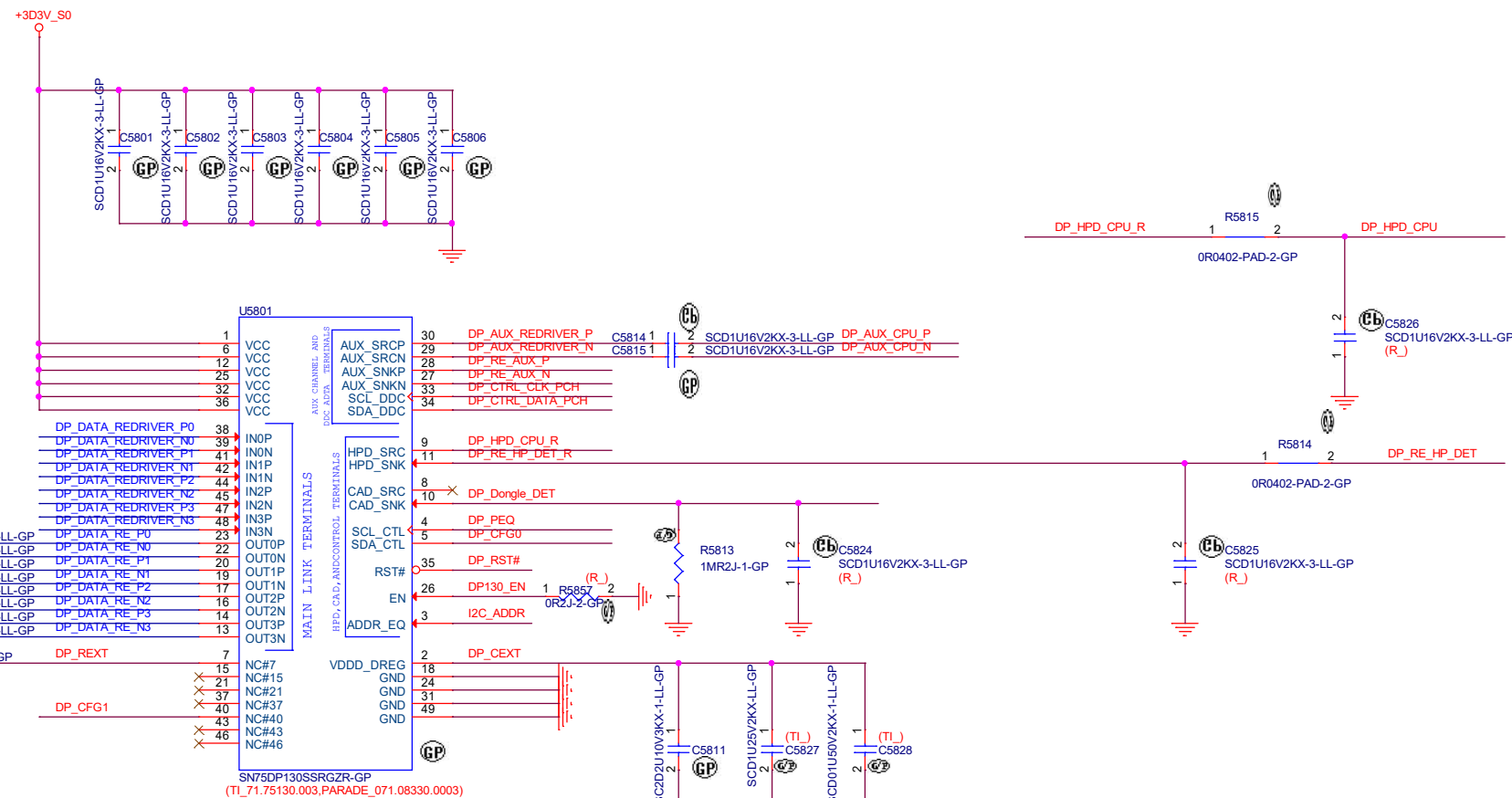
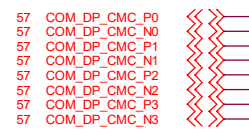
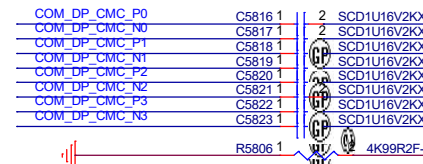
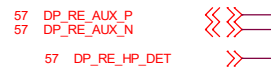
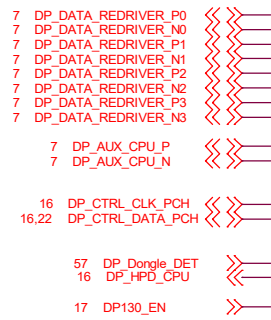
58 COM_DP_CMC_P0
58 COM_DP_CMC_N0
58 COM_DP_CMC_P1
58 COM_DP_CMC_N1
58 COM_DP_CMC_P2
58 COM_DP_CMC_N2
58 COM_DP_CMC_P3
58 COM_DP_CMC_N3

58 DP_RE_AUX_P
58 DP_RE_AUX_N

58 DP_Dongle_DET
58 DP_RE_HP_DET



Link to CPU



D

C

B

A


D

C

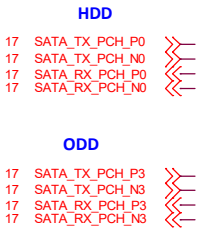
B

A

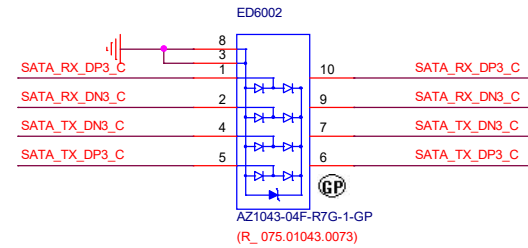
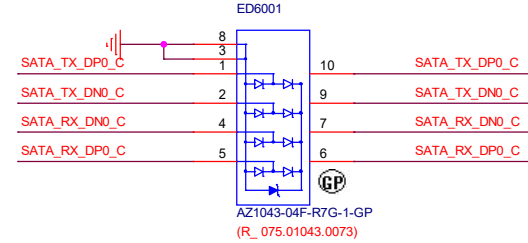
Reserved

| | | | |
|---|---------------------------|---|-----------|
|  | | Wistron Incorporated 12F, 88, Hsin Tai Wu Rd Hsichih, Taipei | |
| Title 059_Display switch_# (R) | | | |
| Size A | Document Number LM820Z | | Rev SA |
| Date: | Thursday, April 19, 2018 | Sheet | 59 of 107 |

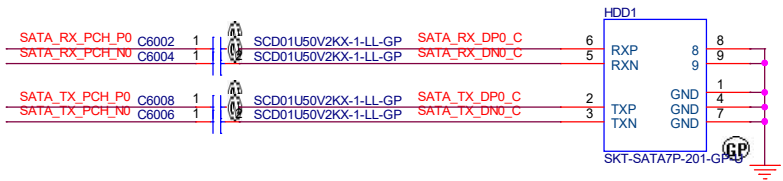
SATA



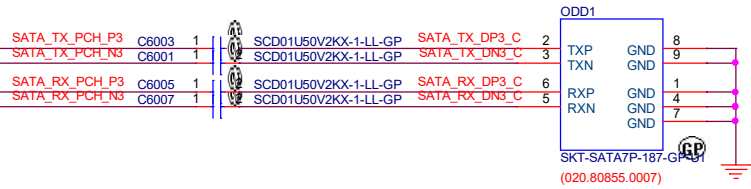
需靠近 CONN



SATA HDD Connector (Red color)

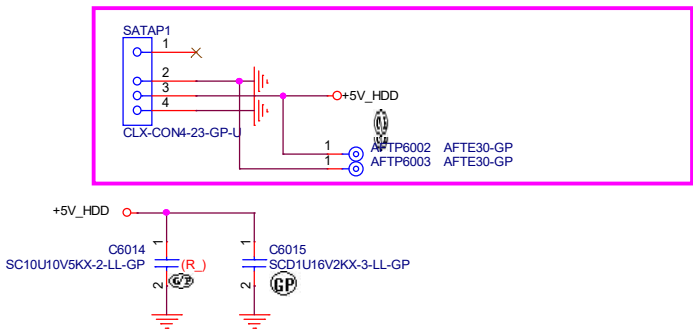


SATA ODD Connector (black color)



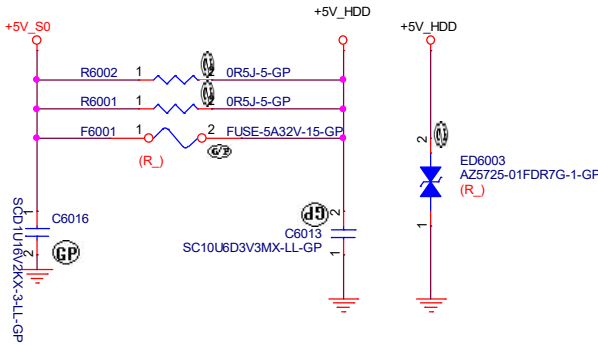
SATA

Layout: Please put them together



AC coupling caps near connector<100 mils

2018.3.29 SVT
unmount F6001, mount R6001 R6002
Sophie



CLINE I2C

17 CLINK_CLK_LAN
17 CLINK_DATA_LAN
17 CLINK_RST_LAN_N

PCIE

16 PCIE_RX_PCH_N8
16 PCIE_RX_PCH_P8
16 PCIE_TX_PCH_N8
16 PCIE_TX_PCH_P8

20,24,31 PCH_WAKE_N
24,31,68,76,91 LRESET_N

USB

16 USB_PCH_PN14
16 USB_PCH_PP14

CLOCK

20 SUSCLK_PCH
18 WLAN_CLK100M_PCH#
18 WLAN_CLK100M_PCH

OTHER

17 MPCIE_DISABLE_N
15 BT_RF_KILL_R_N
20,24 SLP_WLAN_N

18 PEG_CLKREQ3_WLAN_N

CNVi

17 CNV_BRI_DT_R
17 CNV_BRI_RSP
17 CNV_RGI_DT_R
17 CNV_RGI_RSP
17 CNV_MFUART2_RXD
17,22 CNV_MFUART2_TXD
17 CNV_PA_BLANKING

17 CNV_WT_D0N
17 CNV_WT_D0P
17 CNV_WT_D1N
17 CNV_WT_D1P
17 CNV_WT_CLKN
17 CNV_WT_CLKP

17 CNV_WR_D0N
17 CNV_WR_D0P
17 CNV_WR_D1N
17 CNV_WR_D1P
17 CNV_WR_CLKN
17 CNV_WR_CLKP

18 CLKIN_XTAL_LCP_R

20 UART_BT_WAKE_N

20 PCM_CLK
20 PCM_OUT
20 PCM_SYNC
20 PCM_IN

17 CNV1_DET

17 WLAN_USB_DET

2017.08.15 SDV
Add CNVi function
Sophie

To PCH

PD to disable

2017.9.12
SIT modify
Sophie

+3D3V_NGFF_WLAN

+1D8V_VCCPRIM

2017.10.11
SIT Add
Sophie

(Debug Card Side)

(Main Board Side)

LF15V Note:

(1) R21= DY R2458(E51_TXD)

(2) R13= DY R2451(E51_RXD)

WLAN Power Enable

2017.9.29
SIT modify
Sophie

wistron

Wistron Incorporated
12F, 88, Hsin Tai Wu Rd
Hsichih, Taipei

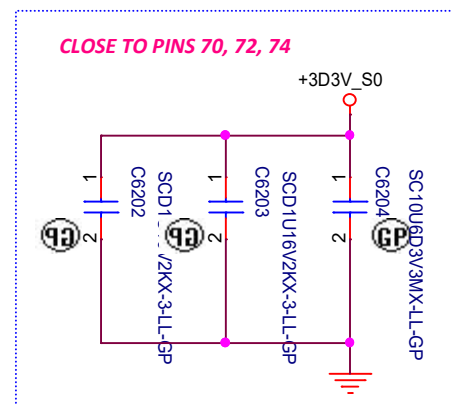
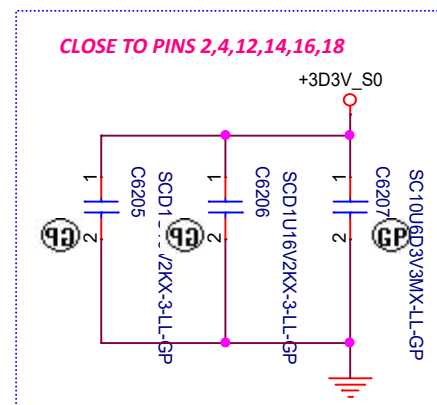
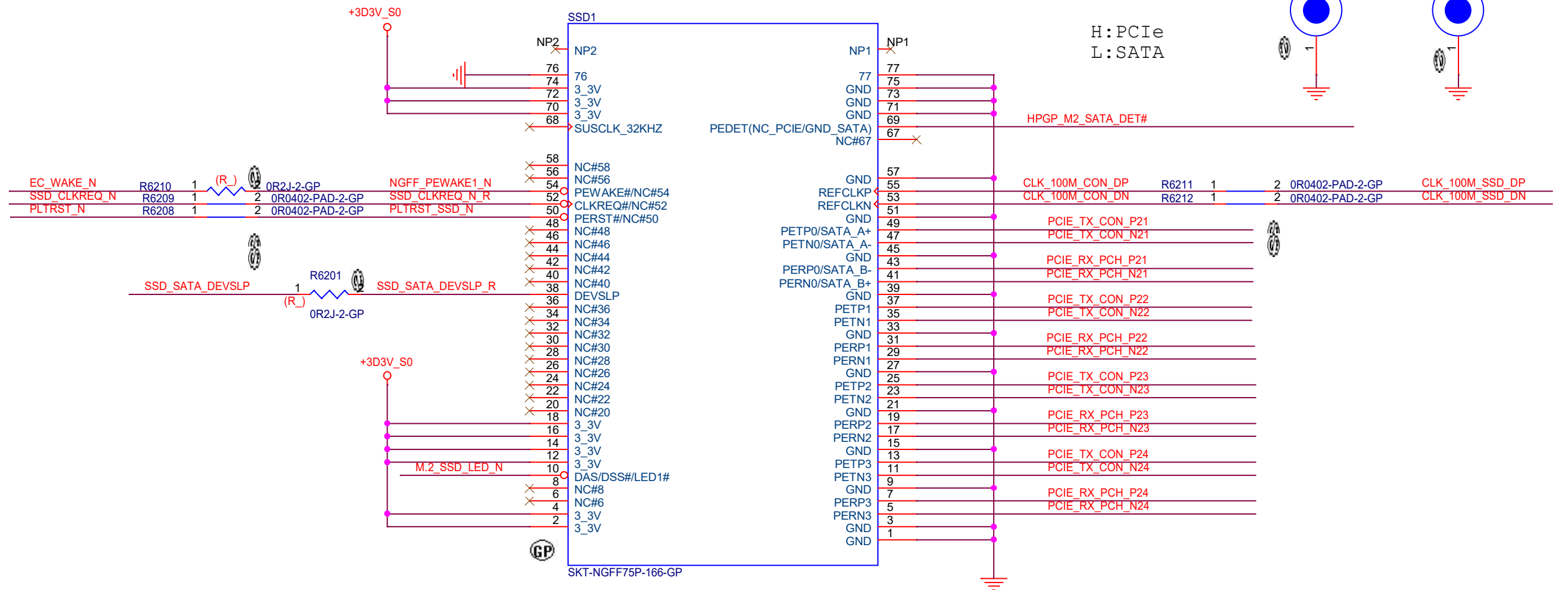
Title
061_Mini card-WLAN

Size
C LM820Z

Date: Thursday, April 19, 2018 Sheet 61 of 107

Rev
SA

NGFF(M Key)



D

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B

A


D

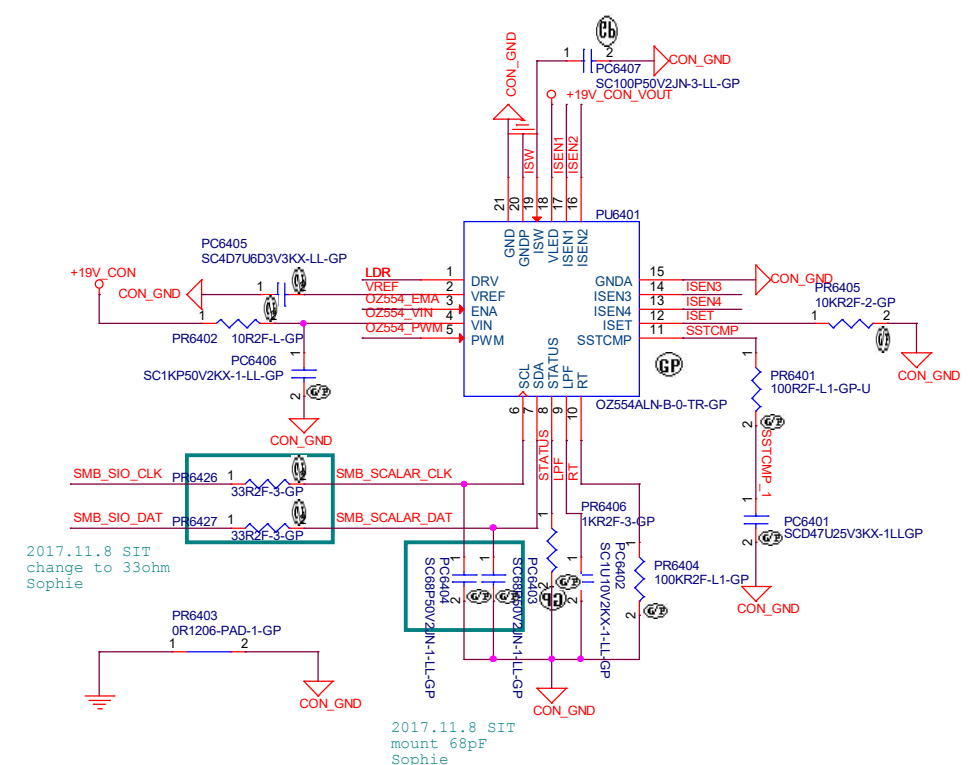
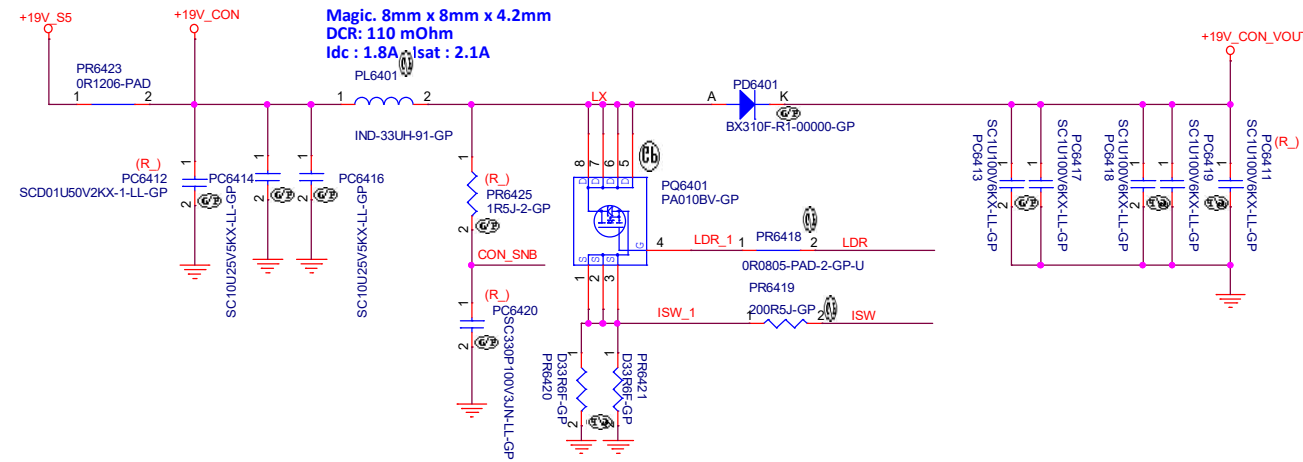
C

B

A

Reserved

| | | | |
|---|---------------------------|---|-----------|
|  | | Wistron Incorporated 12F, 88, Hsin Tai Wu Rd Hsichih, Taipei | |
| Title 063_Mini card-NGFF (R) | | | |
| Size A | Document Number LM820Z | | Rev SA |
| Date: | Thursday, April 19, 2018 | Sheet 63 of 107 | |



24,55 LCD_ID_0
24,55 LCD_ID_1
24,55 LCD_ID_2
24,55 LCD_ID_3

55 RTN1
55 RTN2
55 RTN3
55 RTN4

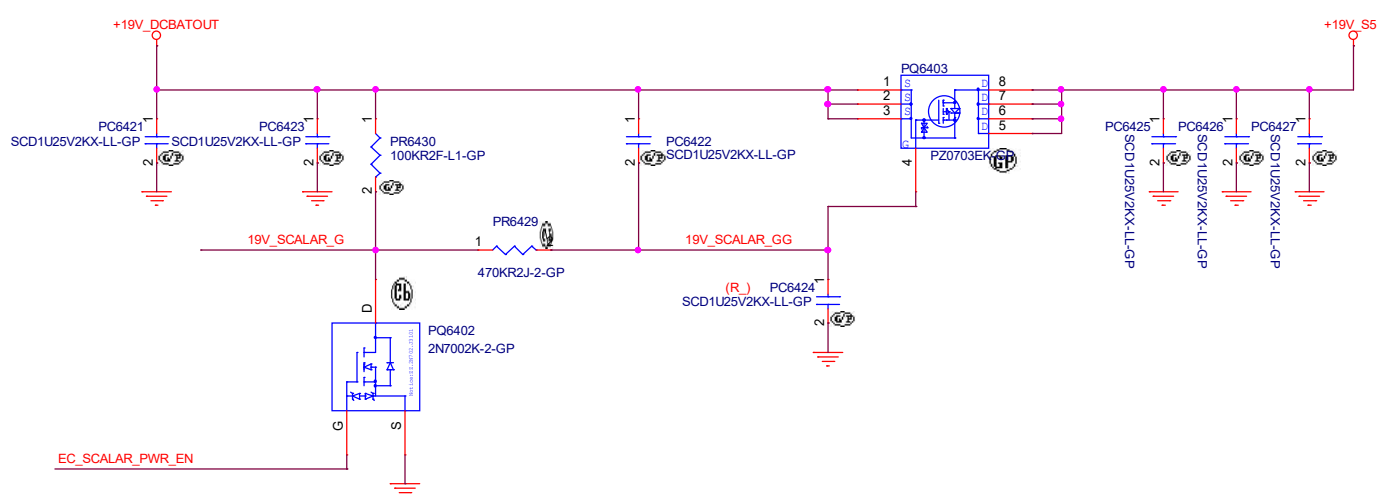
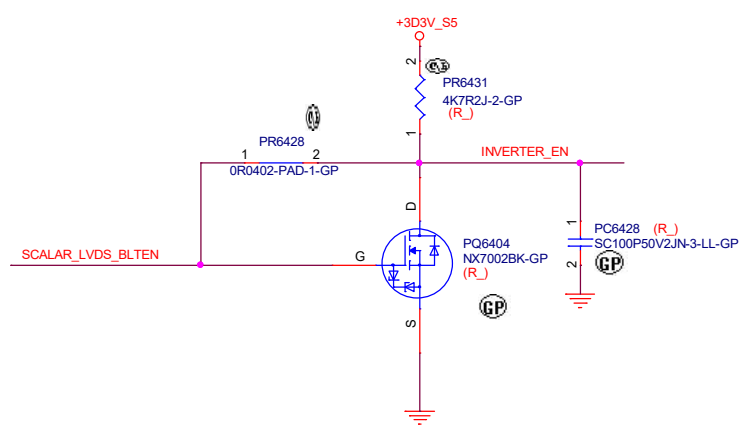
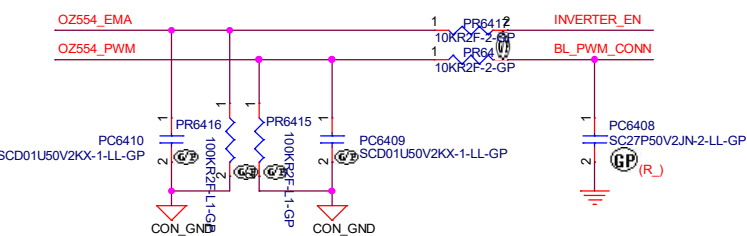
SCALAR and ECIO
24,95 SMB_SIO_CLK
24,95 SMB_SIO_DAT

Panel Control
95 BL_PWM_CONN
24,95 SCALAR_LVDS_BLTEN

24 EC_SCALAR_PWR_EN

LCD_ID_0
LCD_ID_1
LCD_ID_2
LCD_ID_3

ISEN1 PR6407 0R0402-PAD-2-GP RTN1
ISEN2 PR6409 0R0402-PAD-2-GP RTN2
ISEN3 PR6408 0R0402-PAD-2-GP RTN3
ISEN4 PR6410 0R0402-PAD-2-GP RTN4

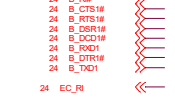


| Panel Model | Cable Spec | | | |
|-------------|------------|-----|-----|------|
| | ID0 | ID1 | ID2 | Vout |
| | 0 | 0 | 0 | |
| | 0 | 0 | 1 | |
| | 0 | 1 | 0 | |
| | 1 | 0 | 0 | |
| | 1 | 1 | 0 | |
| | 1 | 1 | 1 | |

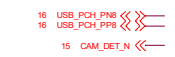
BUTTON BOARD



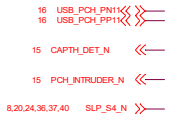
ON BOARD COM PORT



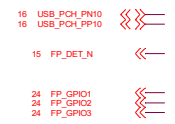
WEBCAM



CAP Touch



FP

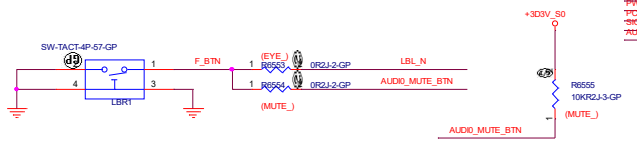


DMIC

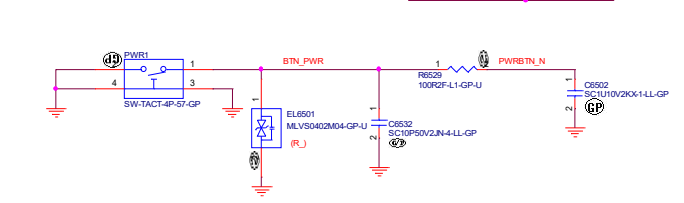


Power button / Low Blue-Ray button/ PWR LED

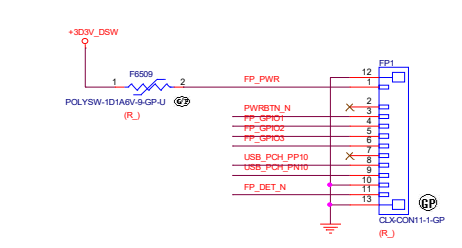
Eye comfort Button



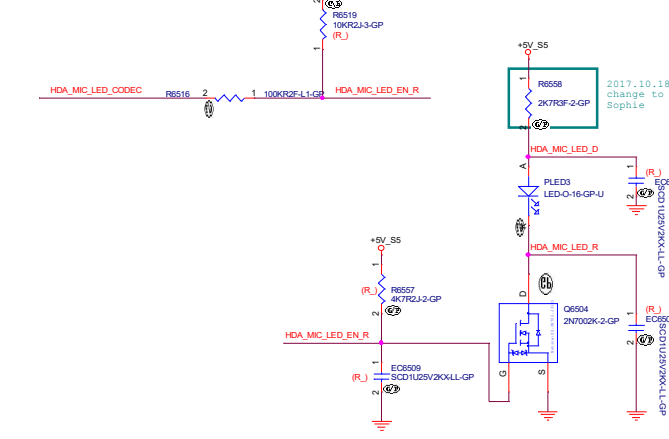
Power Button



Finger printer

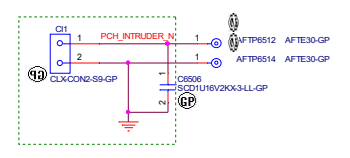


Mic mute LED

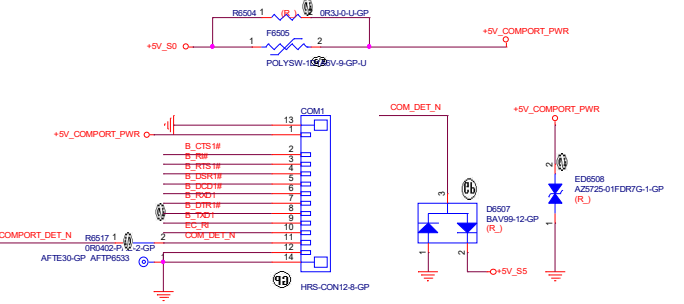


INTRUSION

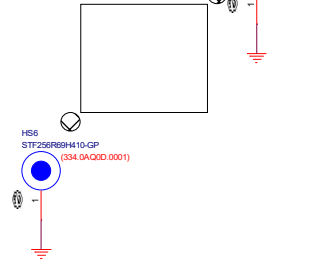
V_3P0_BAT_VREG



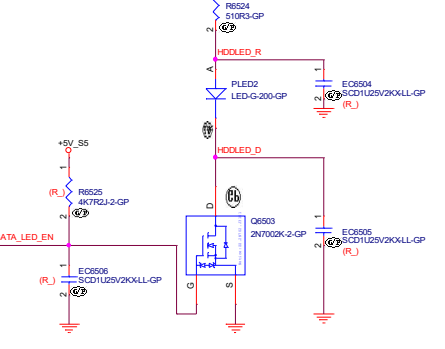
COM



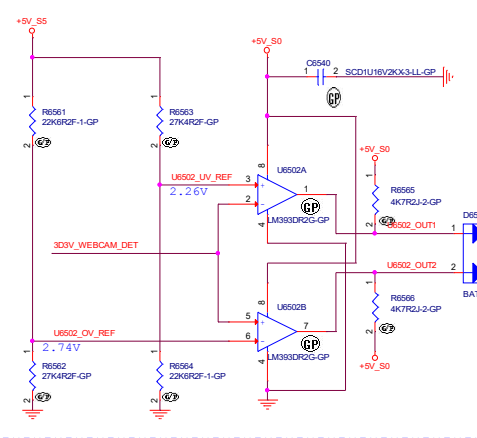
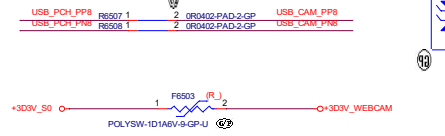
COMFORT SCREW HOLE



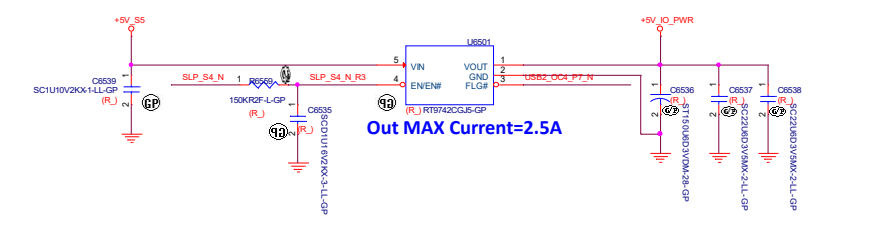
HDD LED



WEBCAM

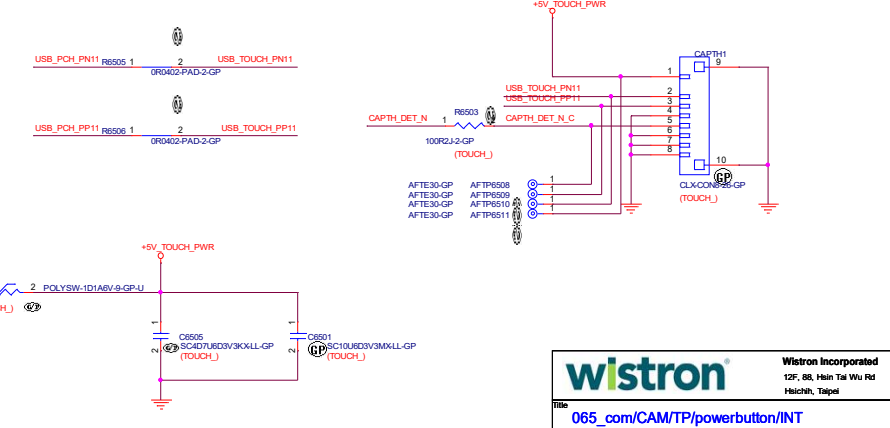
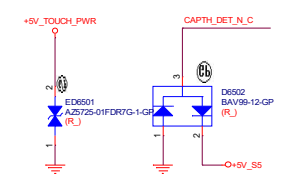


Extended IO



CAP Touch

ESD



| | | | | | | | | | | | | | | | | | | | | | | | | |
|----------|--|--|--|--|---|--|--|--|--|---|--|--|--|--|---|--|--|--|--|---|--|--|--|--|
| 5 | | | | | 4 | | | | | 3 | | | | | 2 | | | | | 1 | | | | |
| Reserved | | | | | | | | | | | | | | | | | | | | | | | | |
| 5 | | | | | 4 | | | | | 3 | | | | | 2 | | | | | 1 | | | | |

</

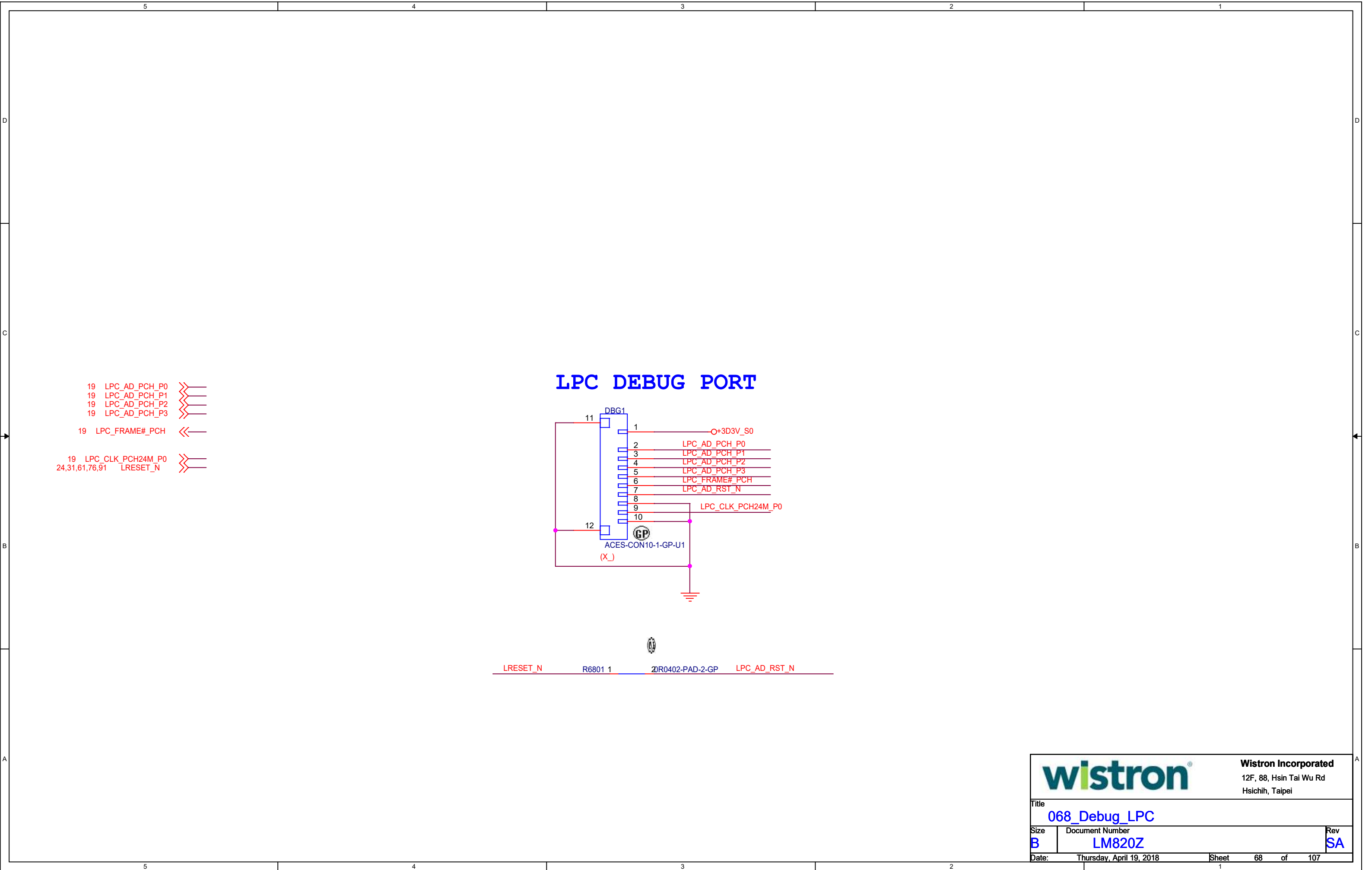
D

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Reserved



wistron®

Wistron Incorporated

12F, 88, Hsin Tai Wu Rd

Hsichih, Taipei

Title

068_Debug_LPC

Size

B

Document Number

LM820Z

Rev

SA

Date:

Thursday, April 19, 2018

Sheet

68

of

107

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Reserved

| | | | |
|---|---------------------------|---|-----------|
|  | | Wistron Incorporated 12F, 88, Hsin Tai Wu Rd Hsichih, Taipei | |
| Title 069_4K Panel (R) | | | |
| Size A | Document Number LM820Z | | Rev SA |
| Date: | Thursday, April 19, 2018 | Sheet 69 of 107 | |

D

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Reserved

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|---|---------------------------|---|-----------|
|  | | Wistron Incorporated 12F, 88, Hsin Tai Wu Rd Hsichih, Taipei | |
| Title 070_G Sensor# (R) | | | |
| Size A | Document Number LM820Z | | Rev SA |
| Date: | Thursday, April 19, 2018 | Sheet | 70 of 107 |

D

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A

Reserved

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|---|---------------------------|---|-----------|
|  | | Wistron Incorporated 12F, 88, Hsin Tai Wu Rd Hsichih, Taipei | |
| Title 071_Thunderbolt_(1/5) (R) | | | |
| Size A | Document Number LM820Z | | Rev SA |
| Date: | Thursday, April 19, 2018 | Sheet | 71 of 107 |

5

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Reserved

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|---|---------------------------|---|-----------|
|  | | Wistron Incorporated 12F, 88, Hsin Tai Wu Rd Hsichih, Taipei | |
| Title 072_Thunderbolt_(2/5) (R) | | | |
| Size A | Document Number LM820Z | | Rev SA |
| Date: | Thursday, April 19, 2018 | Sheet | 72 of 107 |

5

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C

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D

C

B

A

Reserved

| | | | |
|---|---------------------------|---|-----------|
|  | | Wistron Incorporated 12F, 88, Hsin Tai Wu Rd Hsichih, Taipei | |
| Title 073_Thunderbolt_(3/5) (R) | | | |
| Size A | Document Number LM820Z | | Rev SA |
| Date: | Thursday, April 19, 2018 | Sheet | 73 of 107 |

D

C

B

A

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1


D

C

B

A

Reserved

| | | | |
|---|---------------------------|---|-----------------|
|  | | Wistron Incorporated 12F, 88, Hsin Tai Wu Rd Hsichih, Taipei | |
| Title 074_Thunderbolt_(4/5) (R) | | | |
| Size A | Document Number LM820Z | | Rev SA |
| Date: | Thursday, April 19, 2018 | | Sheet 74 of 107 |

5

4

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1

D

C

B

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D

C

B

A

Reserved

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|---|---------------------------|---|-----------|
|  | | Wistron Incorporated 12F, 88, Hsin Tai Wu Rd Hsichih, Taipei | |
| Title 075_Thunderbolt_(5/5) (R) | | | |
| Size A | Document Number LM820Z | | Rev SA |
| Date: | Thursday, April 19, 2018 | Sheet | 75 of 107 |

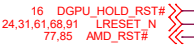
PCIEX8



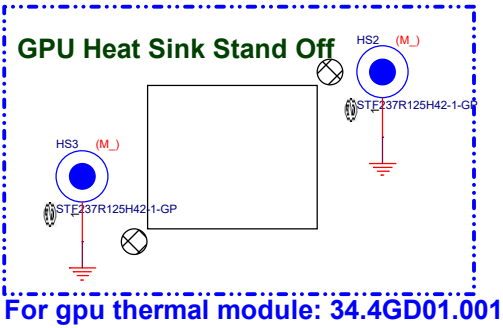
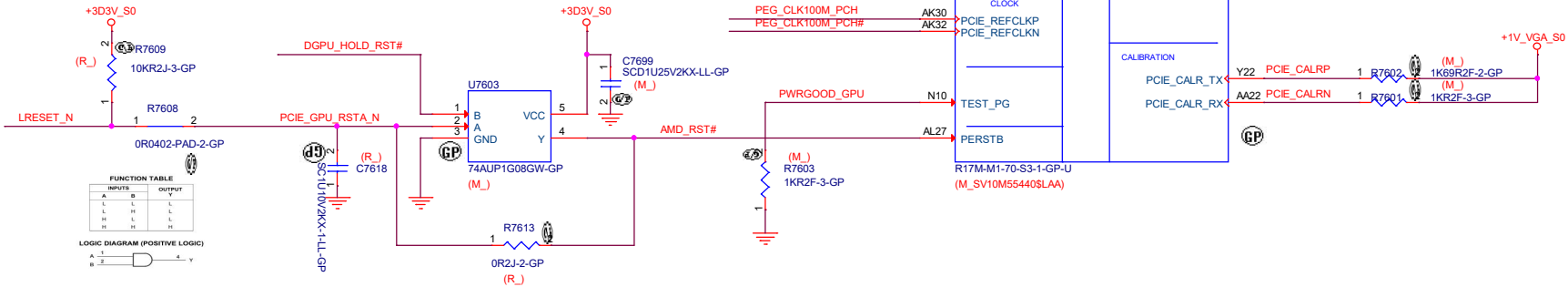
PCI CLK



PCI RESET



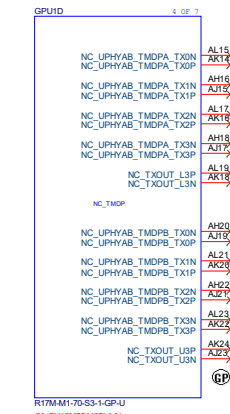
R17M-M1-70 : 071.R17MM.0A0U





NOT FOR PRODUCTION, NO

NC for Topaz and Sun



| MLPS Bit | Strap Name | Description | Description |
|----------|-----------------|----------------------------------|--|
| PS_3[1] | BOARD_CONFIG[0] | Board configuration related | Design dependent, see the description. |
| PS_3[2] | BOARD_CONFIG[1] | strapping, such as for memory ID | |
| PS_3[3] | BOARD_CONFIG[2] | | |
| PS_3[4] | N/A | Reserved. | 1 |
| PS_3[5] | N/A | Reserved. | 1 |

| | |
|--------------------------------|----------------------------------|
| Size D | Document Number LM820Z |
| Date: Thursday, April 19, 2018 | Sheet 77 of 107 |

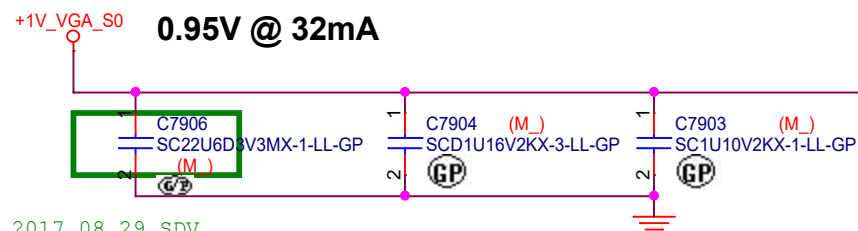
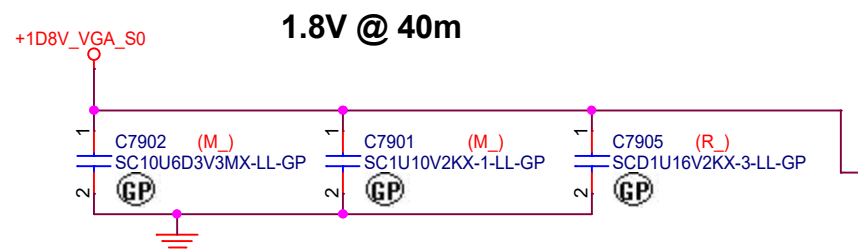
```

81  DQA0_[31..0]  <<—
81  DQA1_[31..0]  <<—
81  DRAM_RST      <<—

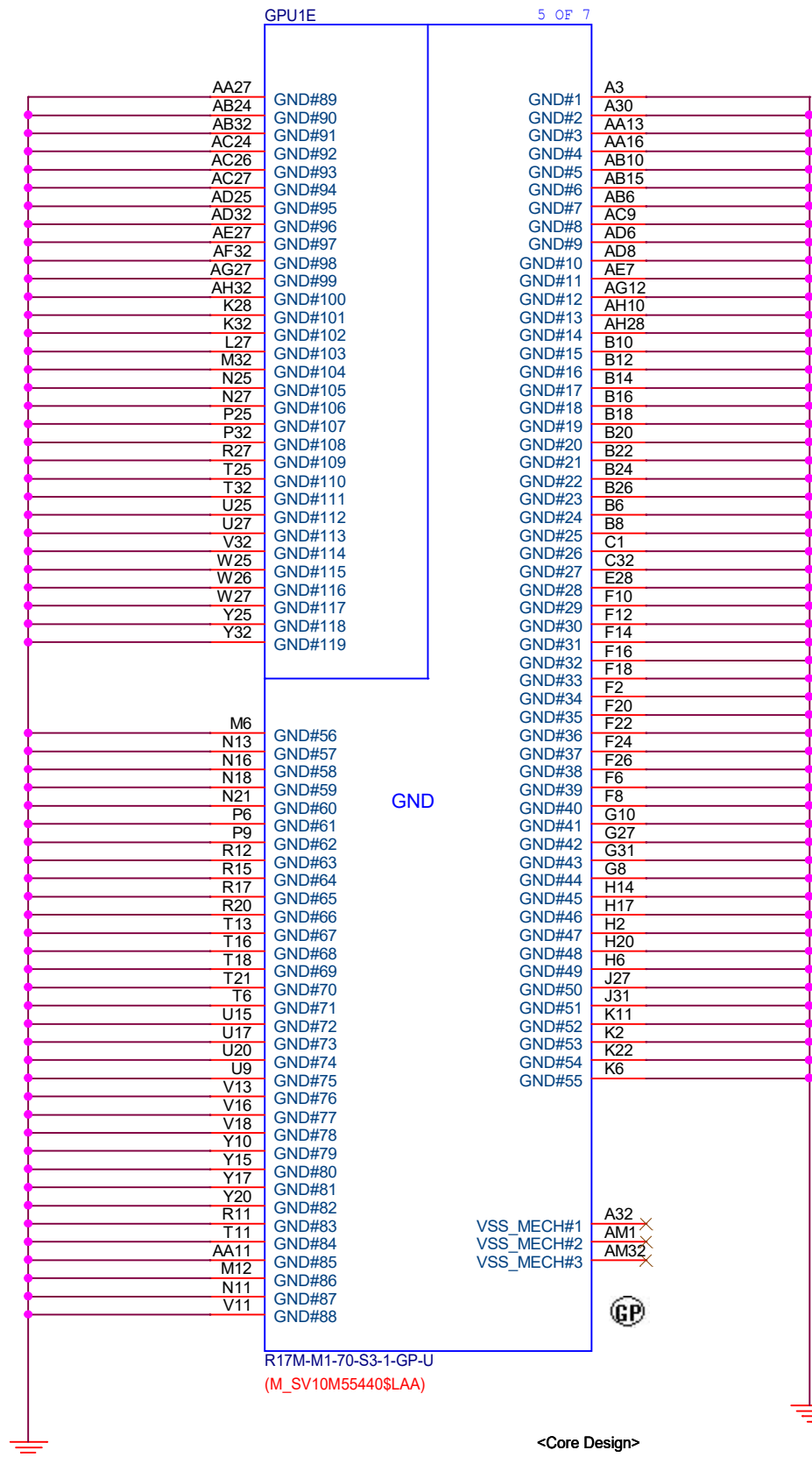
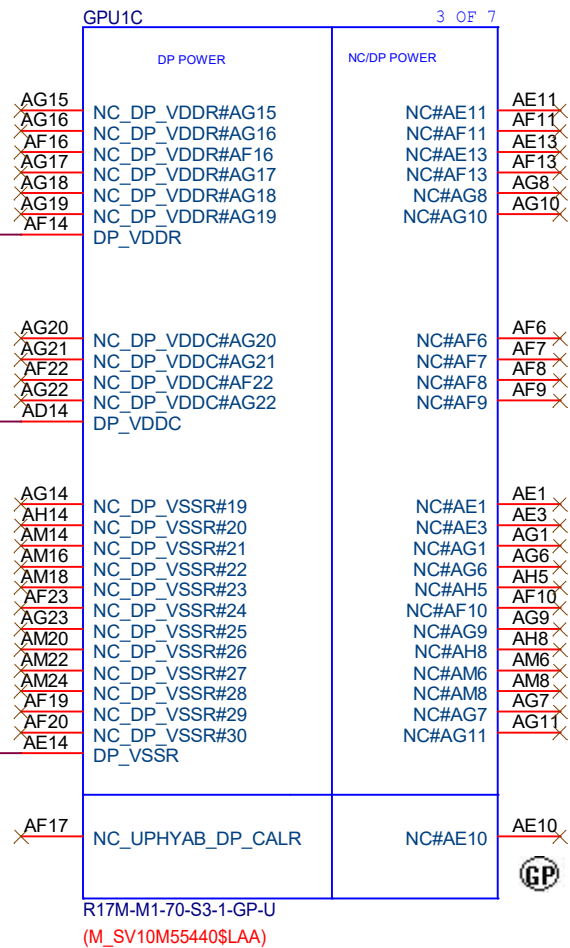
```



1.8V AND 0.95V FOR CLOCK RESOURCE



2017.08.29 SDV
change to 22uF and mount
for power noise
Sophie



<Core Design>

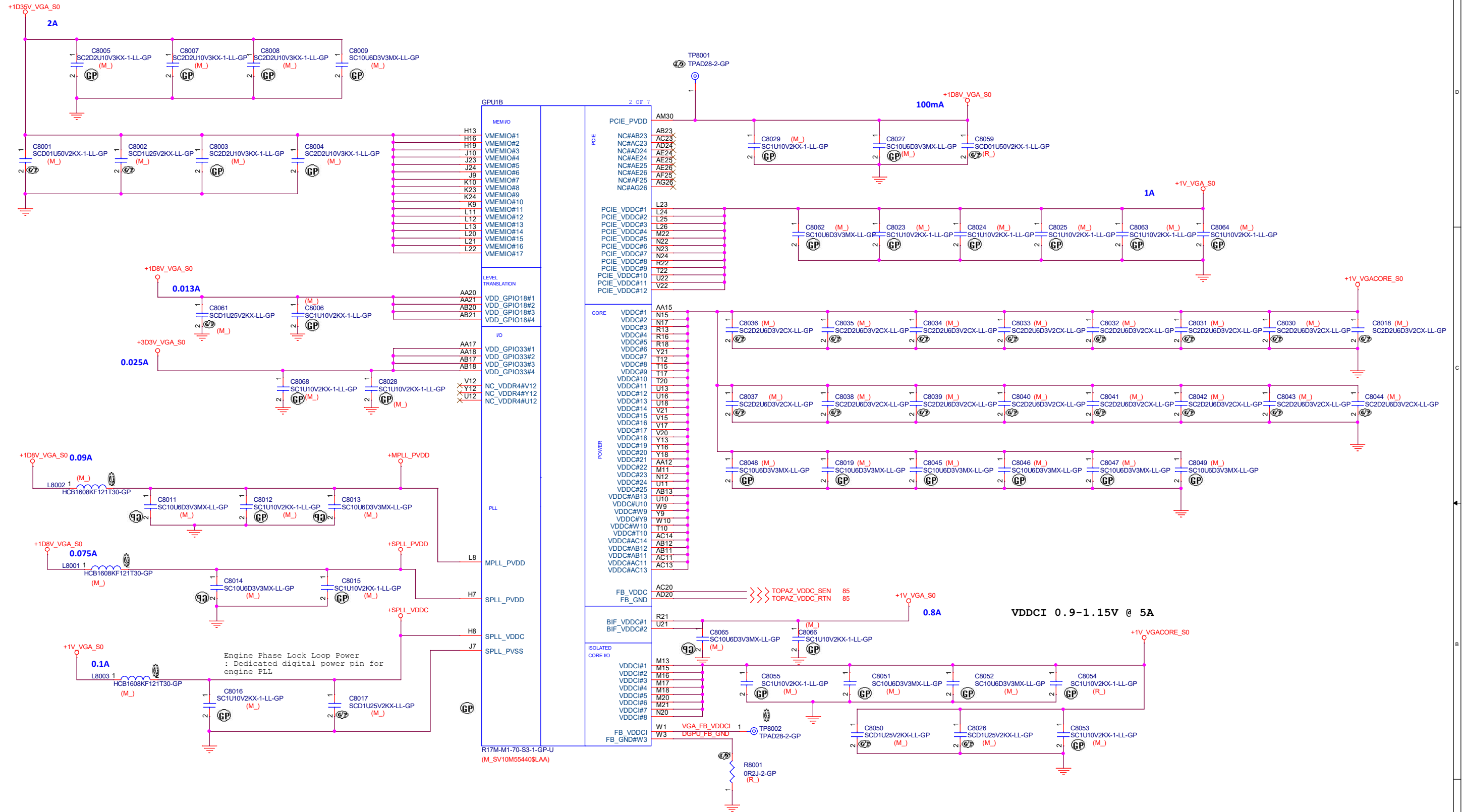
wistron

Wistron Incorporated
21F, 88, Hsin Tai Wu Rd
Hsichih, Taipei

Title **079_GPU (4/5) GPIO/STRAP**

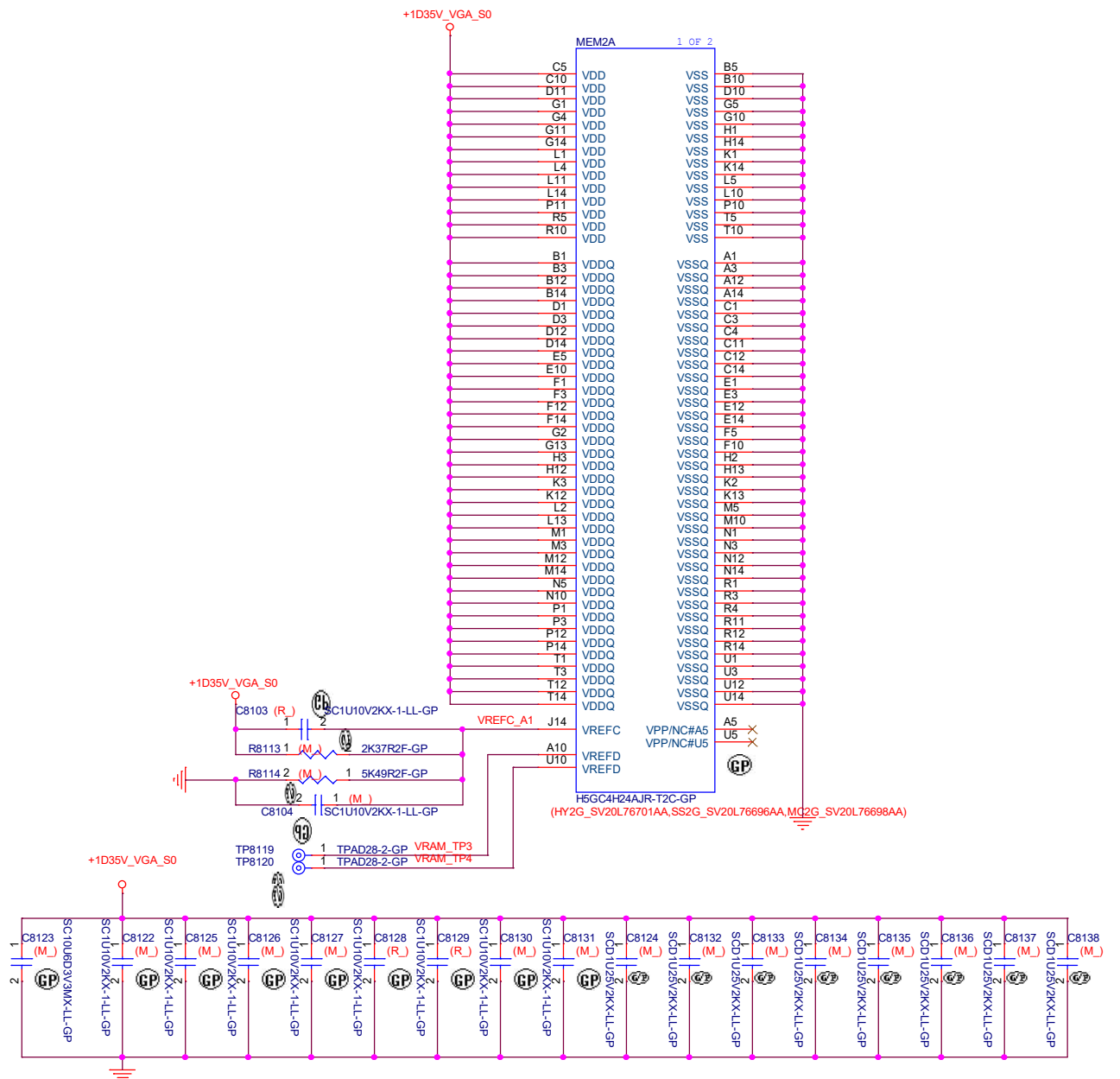
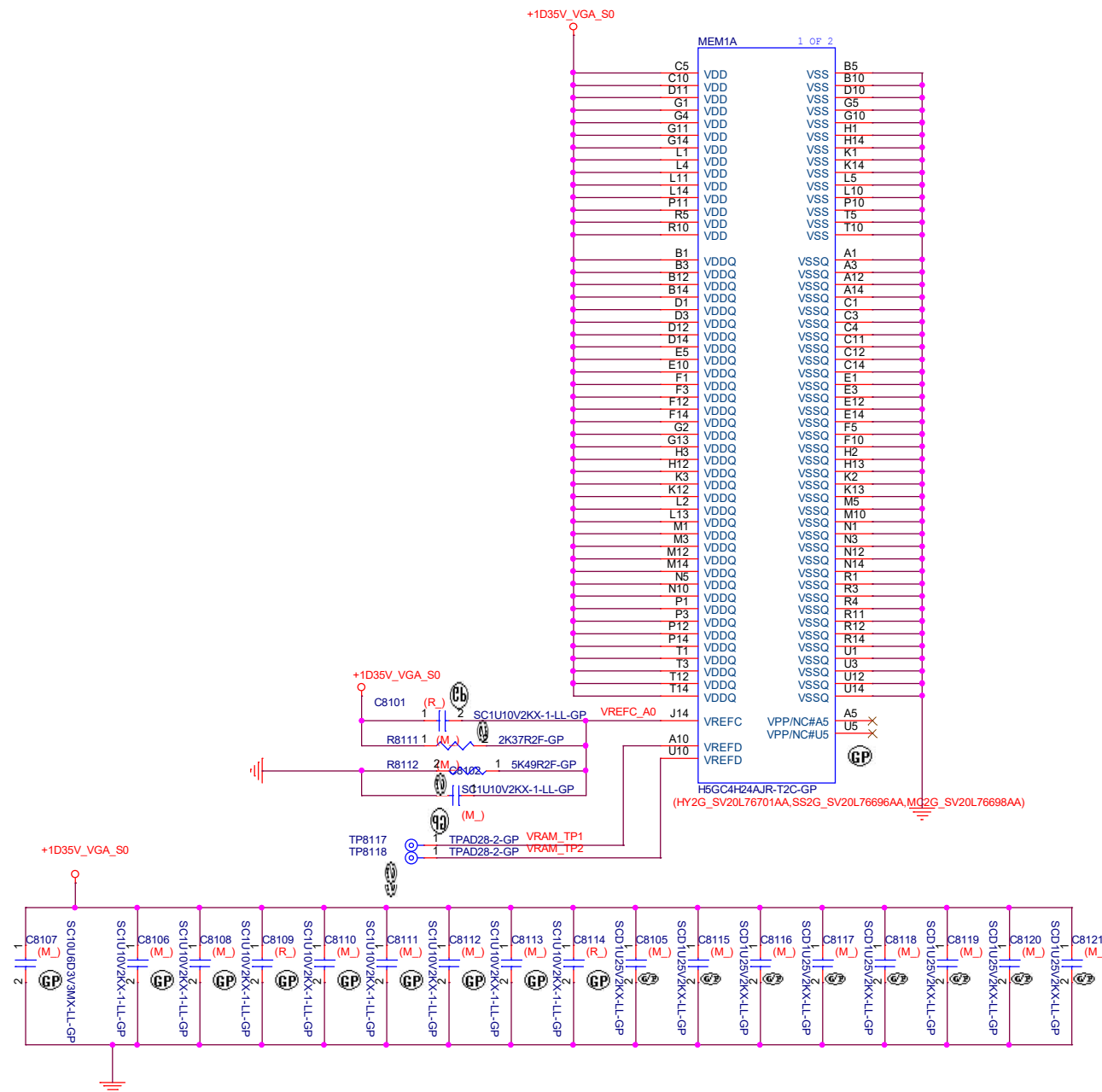
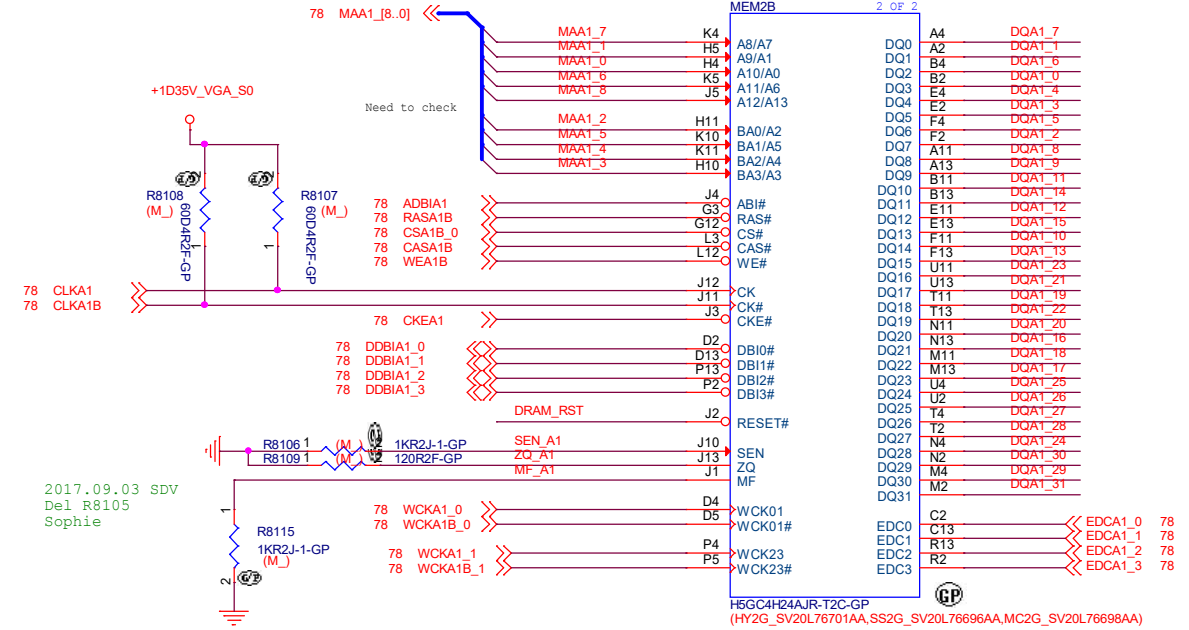
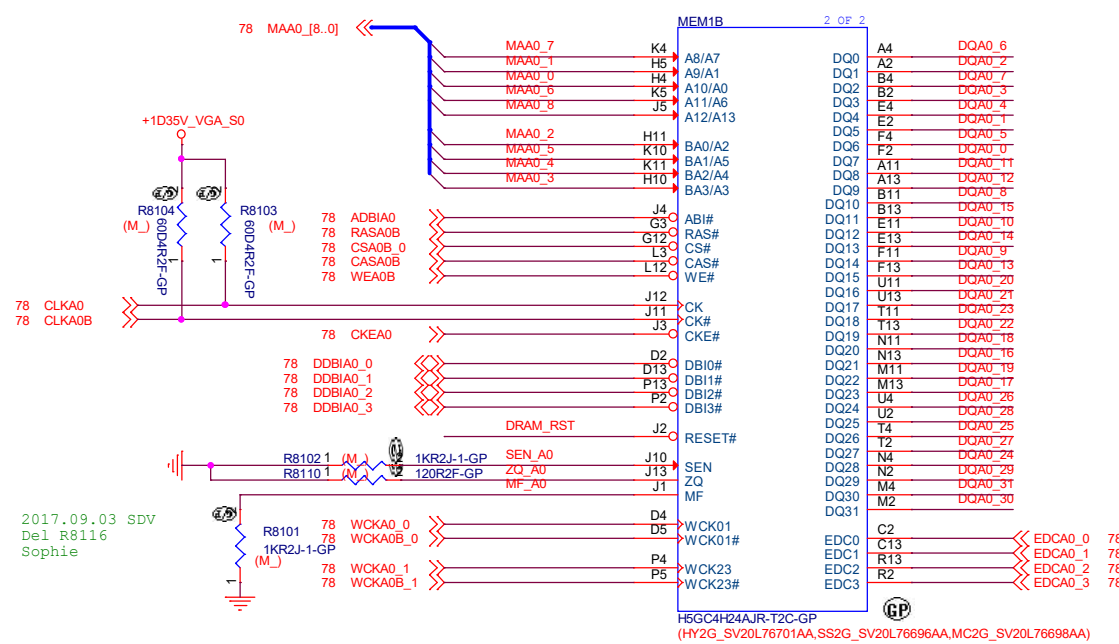
| | | |
|-----------|----------------------------------|------------|
| Size B | Document Number LM820Z | Rev -SA |
|-----------|----------------------------------|------------|

Date: Thursday, April 19, 2018 Sheet 79 of 107



GDDR5 Memory Channel x32 mode

78 DQAO_31..0 >>>
78 DQA1_31..0 >>>
78 DRAM_RST >>>



D

C

B

A

D


C

B

A

Reserved

<Core Design>

| | | | |
|---|----------------------------------|---|------------|
|  | | Wistron Incorporated 21F, 88, Hsin Tai Wu Rd Hsichih, Taipei | |
| Title GPU VRAM_2 (2/4) (R) | | | |
| Size A | Document Number LM820Z | | Rev -SA |
| Date: | Thursday, April 19, 2018 | Sheet 82 of 107 | |

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<Core Design>

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|  | | Wistron Incorporated 21F, 88, Hsin Tai Wu Rd Hsichih, Taipei | |
| Title 083_GPU VRAM_3 (3/4) (R) | | | |
| Size A | Document Number LM820Z | | Rev -SA |
| Date: | Thursday, April 19, 2018 | Sheet 83 of 107 | |

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<Core Design>



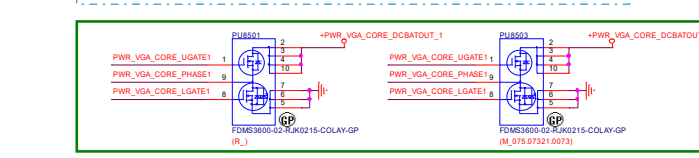
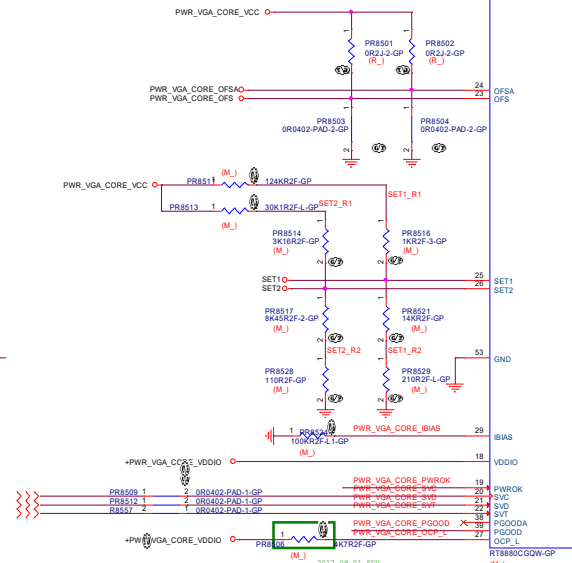
Wistron Incorporated
21F, 88, Hsin Tai Wu Rd
Hsichih, Taipei

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| Title | 084_GPU VRAM_4 (4/4) (R) |
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| Size A | Document Number LM820Z | Rev -SA |
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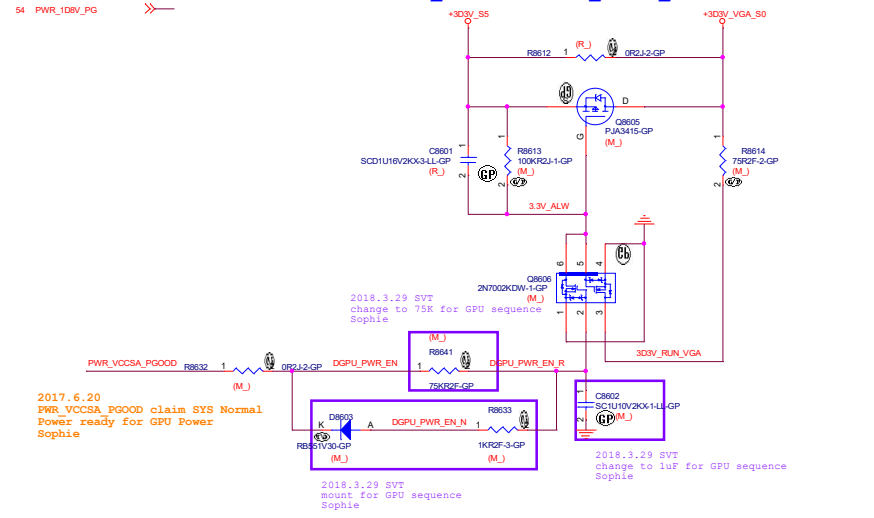
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| Date: | Thursday, April 19, 2018 | Sheet | 84 | of | 107 |
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|------------------------|-------------|---|
| MVDDQ | 1.35 or 1.5 | 0 |
| +1.8V | 1.8 | 0 |
| +0.95V | 0.95 | 0 |
| +3.3V from Motherboard | 3.3 | 0 |

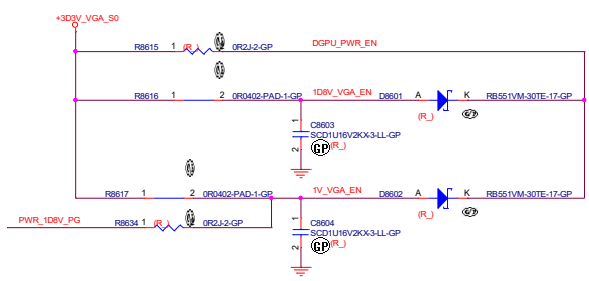


16.85 DGPU_PWR_EN
41.50 PWR_VCCSA_PGOOD
54 PWR_1D8V_PG

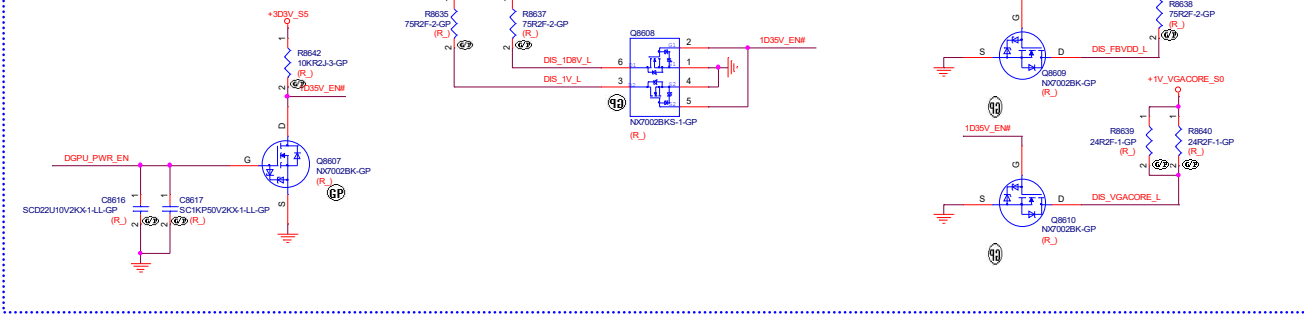
3D3V_S5 to 3D3V_VGA_S0 Transfer



1D05V_VGA 1D8V_VGA



GPU Discharge circuit



GPU PWR Sequencing

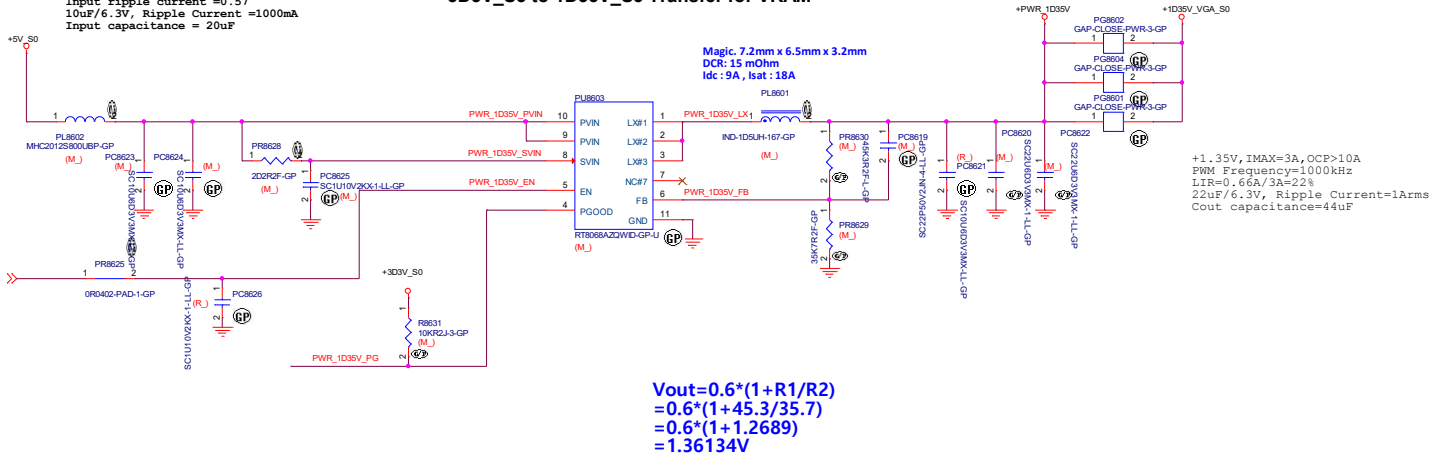
3D3V_VGAS0
=> 0D95V_VGA_S0/1D8V_VGA_S0
=> 1D5V_VGA_S0
=> VGA_CORE

All the ASIC supplies must reach their respective nominal voltages withing **20ms** of the start of the ramp-up sequence, though a shorter ramp-up duration is preferred. The maximum slew rate on all rails is 50mV/us.

It is recommended that the 3.3V rail ramp up first.

It is recommended that the 0.95V rail reach at least 90% of its normal value no later than 2ms from the start of VDDC ramping up.

3D3V_S5 to 1D35V_S5 Transfer for VRAM



$$\begin{aligned} V_{out} &= 0.6 * (1 + R1/R2) \\ &= 0.6 * (1 + 45.3/35.7) \\ &= 0.6 * (1 + 1.2689) \\ &= 1.36134V \end{aligned}$$

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|  | | Wistron Incorporated 21F, 88, Hsin Tai Wu Rd Hsichih, Taipei | |
| Title 087_GPU Switch_(1/2) (R) | | | |
| Size A | Document Number LM820Z | | Rev -SA |
| Date: | Thursday, April 19, 2018 | Sheet 87 of 107 | |

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<Core Design>

wistron

Wistron Incorporated
21F, 88, Hsin Tai Wu Rd
Hsichih, Taipei

Title

088_GPU Switch_(2/2) (R)

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Document Number

LM820Z

Rev

-SA

Date:

Thursday, April 19, 2018

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|  | | | | | | | | | | Wistron Incorporated 21F, 88, Hsin Tai Wu Rd Hsichih, Taipei | | | | | | | | | | | | | | |
| Title | | | | | | | | | | 088_GPU Switch_(2/2) (R) | | | | | | | | | | | | | | |
| Size A | | | | | Document Number LM820Z | | | | | | | | | | | | | | | Rev -SA | | | | |
| Date: | | | | | | | | | | Thursday, April 19, 2018 | | | | | | | | | | Sheet 88 of 107 | | | | |

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|  | | Wistron Incorporated 12F, 88, Hsin Tai Wu Rd Hsichih, Taipei | |
| Title 089_GPU others (R) | | | |
| Size A | Document Number LM820Z | | Rev -1 |
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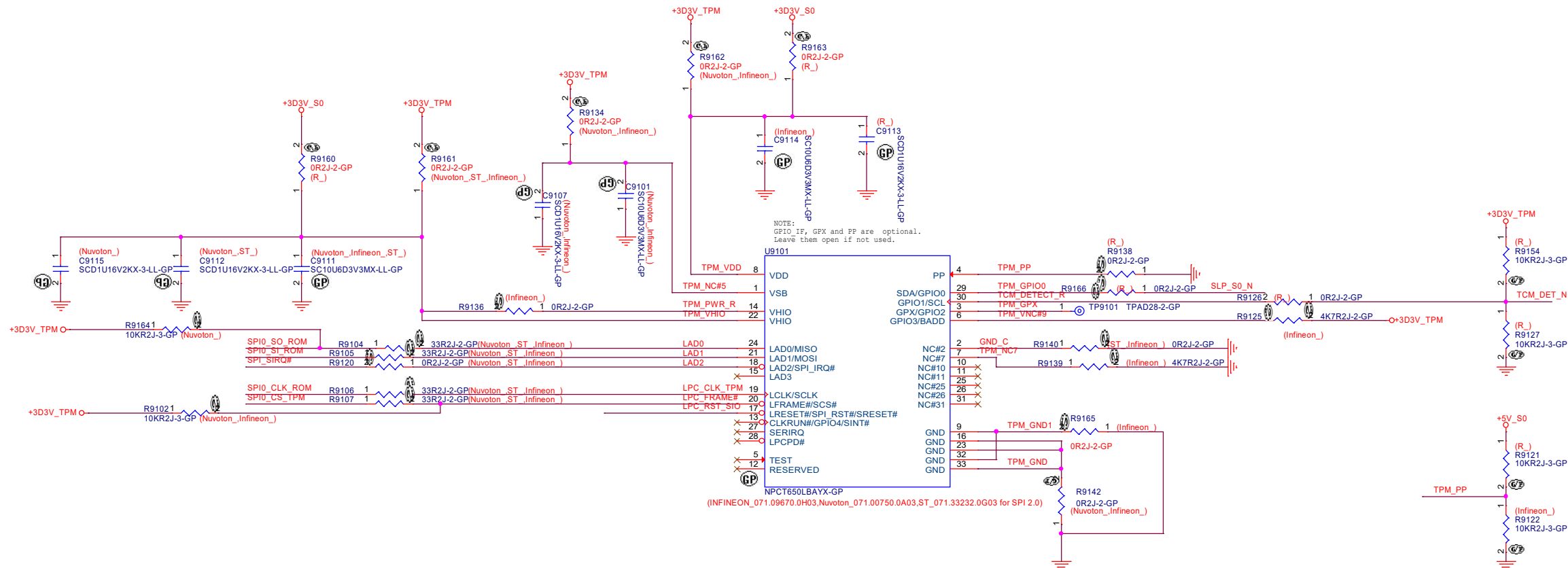
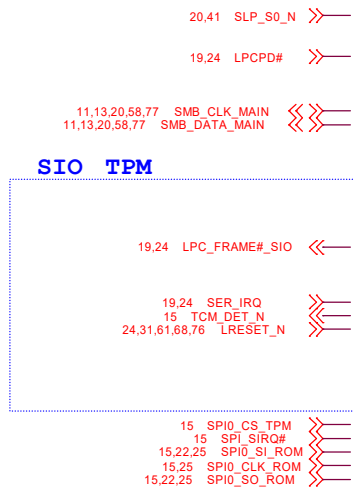
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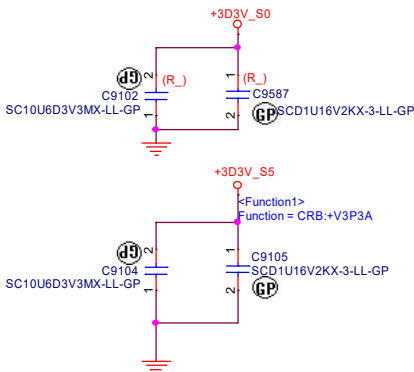
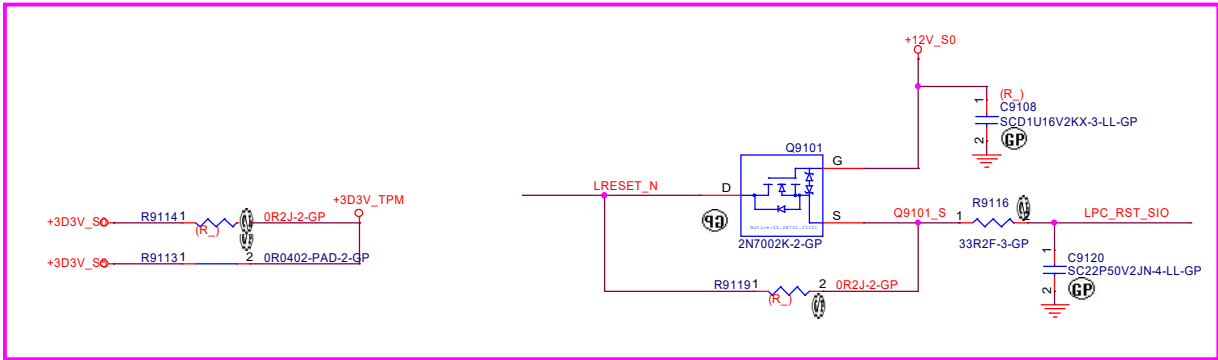
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|  | | Wistron Incorporated 12F, 88, Hsin Tai Wu Rd Hsichih, Taipei | |
| Title 090_NFC (R) | | | |
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TPM PIN DEFINE

| Vendor | Nuvoton | ST | Infineon | Lenovo design |
|---------|-----------------------|------------------|--------------|-----------------------|
| PN | NPCT750x | ST33HTPH2E32AHB4 | SLB9670VQ2.0 | Colay 3 vendors |
| Package | VQFN32, SPI interface | | | |
| Pin1 | VSB | NiC | NCI/VDD | Nuvoton,Infineon VDD |
| Pin2 | NC1 | GND | GND | Infineon, ST GND |
| Pin3 | NC2 | NiC | NCI | Connect to test point |
| Pin4 | PP/GPIO6 | NiC | NCI | NC |
| Pin5 | NC3 | NiC | NCI | NC |
| Pin6 | GPIO3 | NC | GPIO | Infineon PU 4.7K |
| Pin7 | NC4 | PP | PP | Infineon PD 4.7K |
| Pin8 | VHIO1 | NiC | VDD | Nuvoton,Infineon VDD |
| Pin9 | NC5 | NiC | GND | Infineon GND |
| Pin10 | NC6 | NiC | NCI | NC |
| Pin11 | NC7 | NiC | NCI | NC |
| Pin12 | NC8 | NiC | NCI | NC |
| Pin13 | GPIO4/SINT# | NiC | NCI | NC |
| Pin14 | NC9 | NiC | NCI/VDD | Infineon VDD |
| Pin15 | NC10 | NiC | NCI | NC |
| Pin16 | GND1 | NiC | NCI/GND | Nuvoton,Infineon GND |
| Pin17 | RESET# | SPI_RST# | RST# | RST# |
| Pin18 | SPI_IRQ#/GPIO2 | SPI_PIRQ# | PIRQ# | PIRQ# |
| Pin19 | SCLK | SPI_CLK | SCLK | SCLK |
| Pin20 | SCS#/GPIO5 | SPI_CS# | CS# | CS# |
| Pin21 | MOSI/GPIO7 | MOSI | MOSI | MOSI |
| Pin22 | VHIO2 | VPS | VDD | VDD |
| Pin23 | GND2 | NiC | GND | Nuvoton,Infineon GND |
| Pin24 | MISO | MISO | MISO | MISO |
| Pin25 | NC11 | NiC | NCI | NC |
| Pin26 | NC12 | NiC | NCI | NC |
| Pin27 | NC13 | NiC | NCI | NC |
| Pin28 | NC14 | NiC | NCI | NC |
| Pin29 | SDA/GPIO0 | NiC | NC | NC |
| Pin30 | SCL/GPIO1 | NiC | NC | NC |
| Pin31 | NC15 | NiC | NCI | NC |
| Pin32 | NC16 | NiC | GND | Infineon GND |



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|  | | Wistron Incorporated 12F, 88, Hsin Tai Wu Rd Hsichih, Taipei | |
| Title 092_PS2 (R) | | | |
| Size A | Document Number LM820Z | | Rev SA |
| Date: | Thursday, April 19, 2018 | Sheet | 92 of 107 |

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|  | | Wistron Incorporated 12F, 88, Hsin Tai Wu Rd Hsichih, Taipei | |
| Title 093_Express Card# (R) | | | |
| Size A | Document Number LM820Z | | Rev SA |
| Date: | Thursday, April 19, 2018 | | Sheet 93 of 107 |

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|  | | Wistron Incorporated 12F, 88, Hsin Tai Wu Rd Hsichih, Taipei | |
| Title 094_Smart Card# (R) | | | |
| Size A | Document Number LM820Z | | Rev SA |
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|  | | Wistron Incorporated 12F, 88, Hsin Tai Wu Rd Hsichih, Taipei | |
| Title 096_MCU# (R) | | | |
| Size A | Document Number LM820Z | | Rev SA |
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|  | | Wistron Incorporated 12F, 88, Hsin Tai Wu Rd Hsichih, Taipei | |
| Title 098_LAN Switch# (R) | | | |
| Size A | Document Number LM820Z | | Rev SA |
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XDP (CPU)


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|  | | Wistron Incorporated 12F, 88, Hsin Tai Wu Rd Hsichih, Taipei | |
| Title 099_XDP&ITP# (R) | | | |
| Size A | Document Number LM820Z | | Rev SA |
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LABEL




LAN ID: FB0F4105E89A




LAN ID: FB0F4105E89A



LAN ID: FB0F4105E89A



LAN ID: FB0F4105E89A



LAN ID: FB0F4105E89A

LBL1
LABEL
(40.3KR24.011)

LBL2
LABEL
(R_)

LBL3
LABEL
(R_)


LBL4
LABEL
(R_340.03203.0001)

LBL5
LABEL
(R_45.3E702.001)

MB serial NO# and MAC address
40.3KR24.011 -> 35 x 15mm
45.41107.011 -> 70 x 8mm
45.41115.001 -> 34 x 13.5mm for aDallas

MB FRU PN Label
340.03203.0001 -> 26 x 11mm
340.03204.0001 -> 31.8 x 4.6mm

Battery Symbol

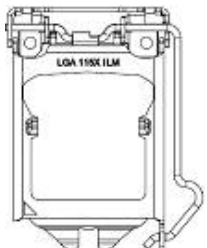


BTT2
BATTERY CR2032
(23.20023.001)

Vendor
P/N:
23.20023.001

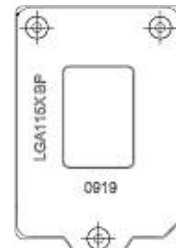
Combination:
U1 + SKT1 + SKT2 + SKT3
062.10015.0081 (FOXCONN) + 22.78003.051 (LOTES) + 022.70001.0121 (LOTES) + 22.78005.281 (FOXCONN)

SKT1




Load Plate
(22.78003.051)

SKT2



Back Plate
(022.70001.0121)

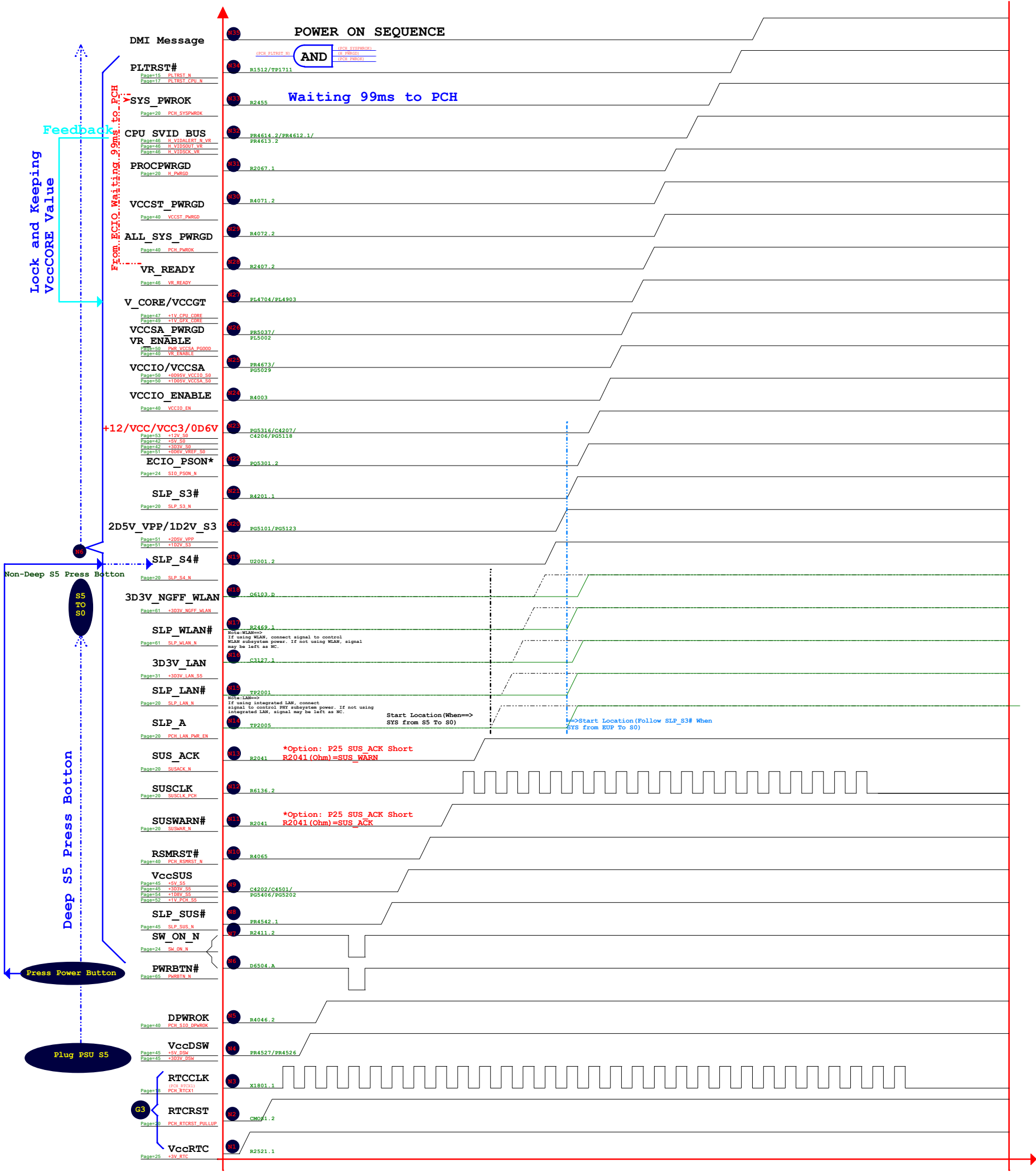
SKT3

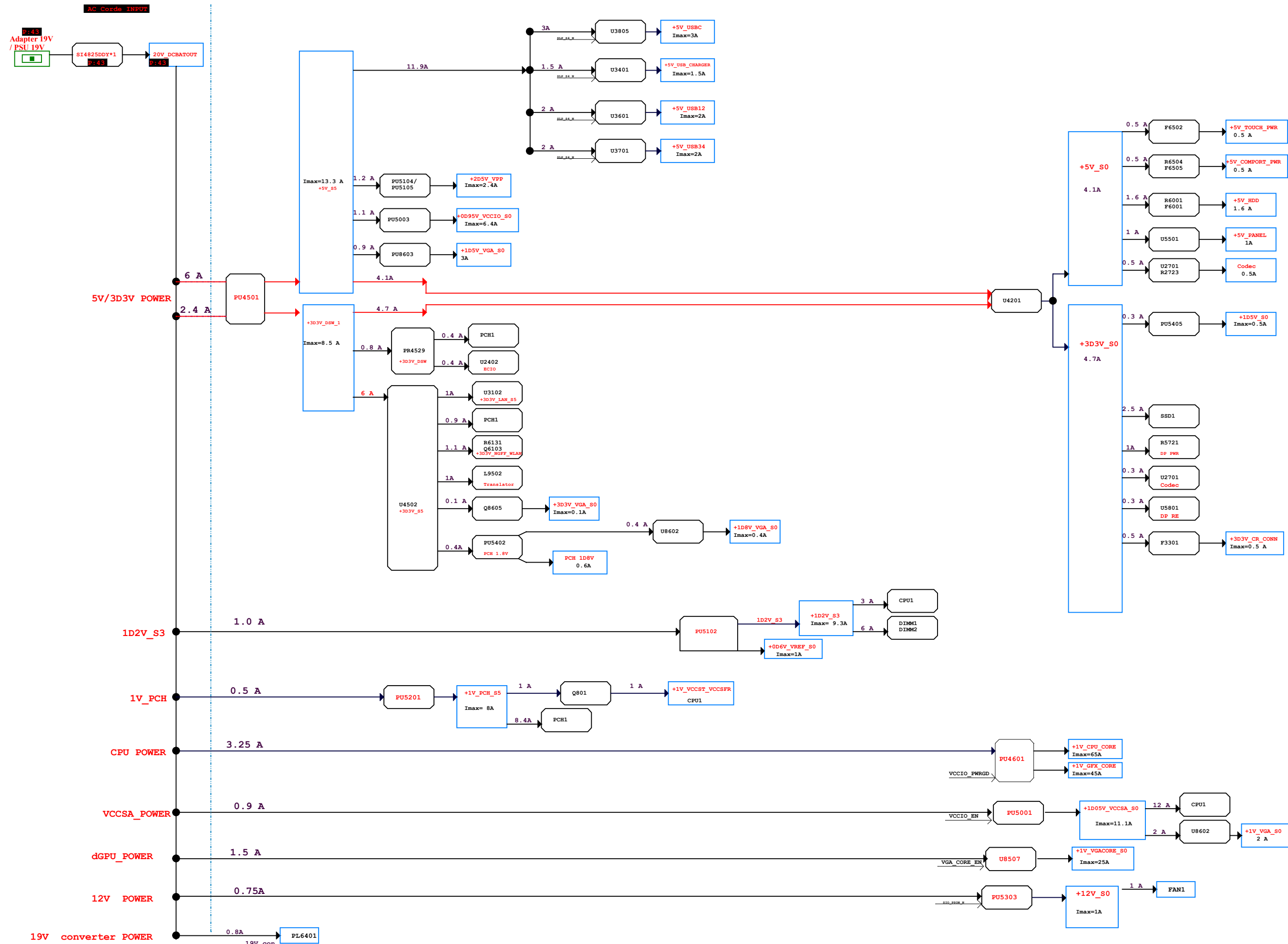


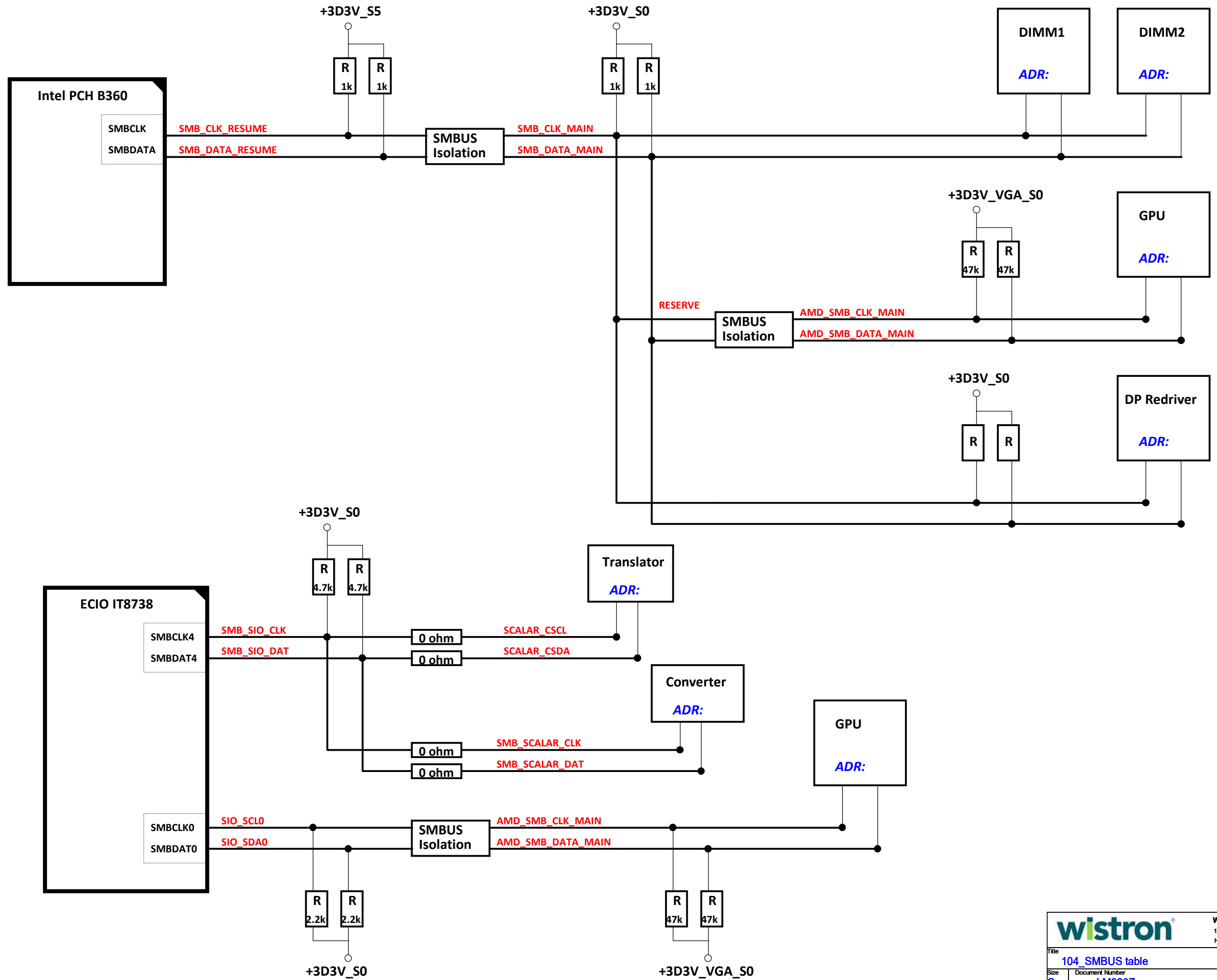
ILMCOVER
(22.78005.171)

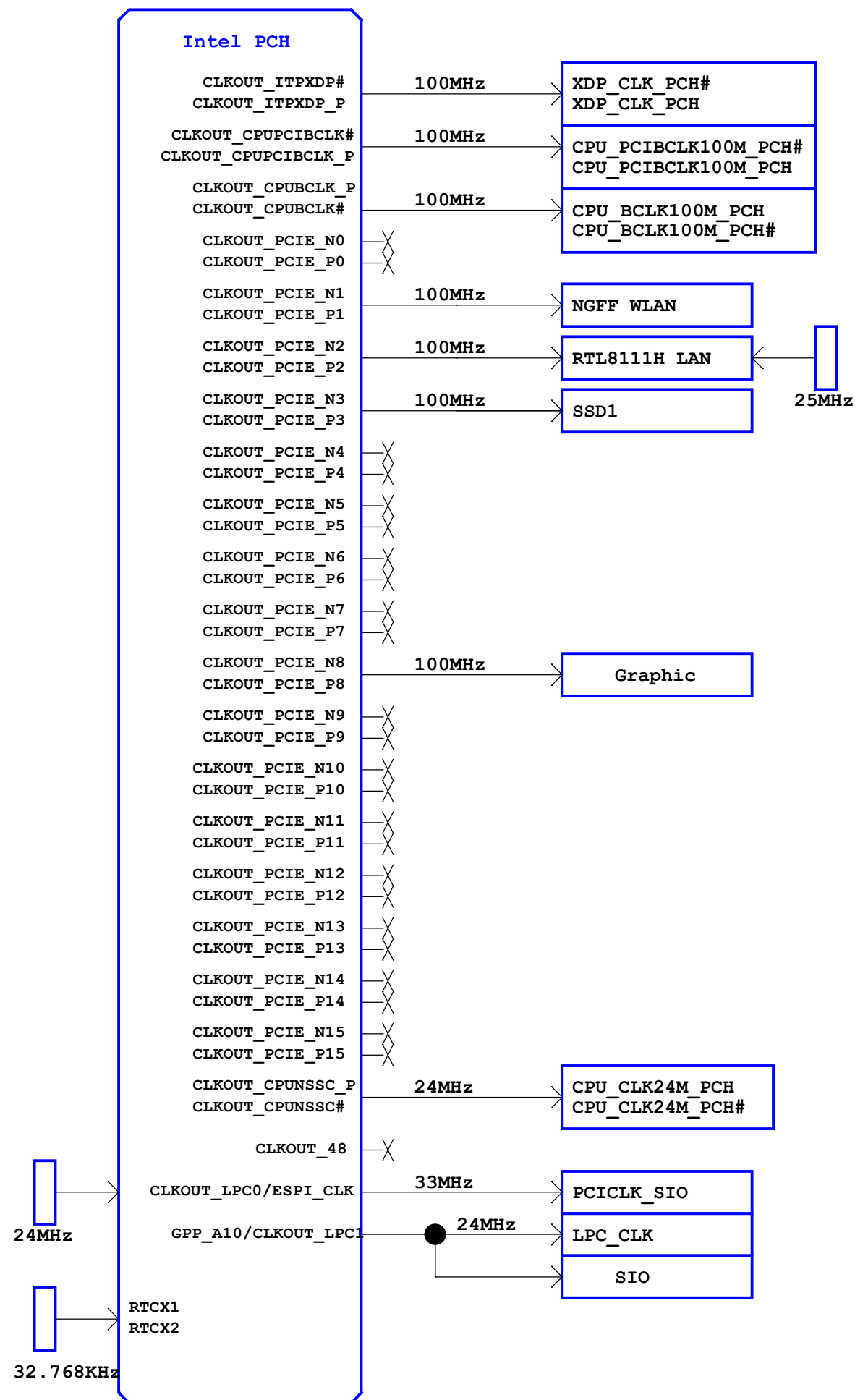
[illegible]

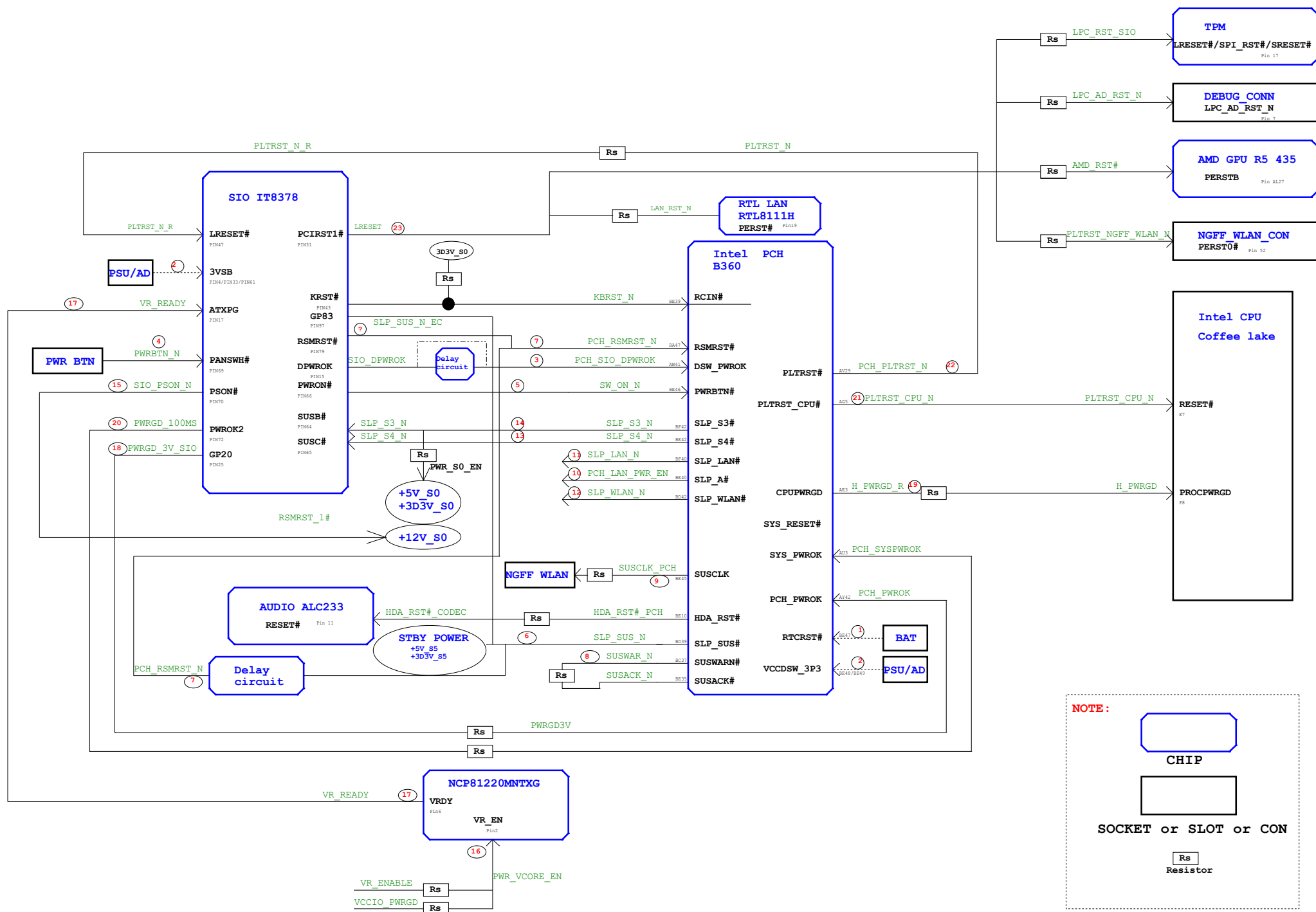
| CNCI (CI) report information | | | | | | | | Project Definition | | | | | | | | | | | | |
|------------------------------|-----------|--|--------------------|--------|-----------|--------|-----------------------------|-----------------------------|-----------|------------------|-------------|----------------|-------------|----------------|-------------|----------------|-------------|-----------|--|-------|
| Ref. No. | Ref. Name | Description (Challenge type) | Technical Solution | Type | Phase End | Status | Impact/Ref. (Ref. ID) | Key Topics (Impact/Ref. ID) | | | | | | | | | | MIS/CI/CI | | Notes |
| | | | | | | | | Ref. No. | Ref. Name | Ref. Description | Ref. Status | Ref. Phase End | Ref. Status | Ref. Phase End | Ref. Status | Ref. Phase End | Ref. Status | | | |
| MIS | SPR-0101 | Natural PLSA - 100% Digital Challenge: not more than 100% digital | Natural PLSA | TLO/OT | MIS/CI/CI | YES | Natural PLSA - 100% Digital | Ref. No. | Ref. Name | Ref. Description | Ref. Status | Ref. Phase End | Ref. Status | Ref. Phase End | Ref. Status | Ref. Phase End | Ref. Status | | | |
| | | | | | | | | Ref. No. | Ref. Name | Ref. Description | Ref. Status | Ref. Phase End | Ref. Status | Ref. Phase End | Ref. Status | Ref. Phase End | Ref. Status | | | |
| MIS | SPR-0102 | Natural PLSA - 100% Digital Challenge: not more than 100% digital | Natural PLSA | TLO/OT | MIS/CI/CI | YES | Natural PLSA - 100% Digital | Ref. No. | Ref. Name | Ref. Description | Ref. Status | Ref. Phase End | Ref. Status | Ref. Phase End | Ref. Status | Ref. Phase End | Ref. Status | | | |
| | | | | | | | | Ref. No. | Ref. Name | Ref. Description | Ref. Status | Ref. Phase End | Ref. Status | Ref. Phase End | Ref. Status | Ref. Phase End | Ref. Status | | | |
| MIS | SPR-0103 | Natural PLSA - 100% Digital Challenge: not more than 100% digital | Natural PLSA | TLO/OT | MIS/CI/CI | YES | Natural PLSA - 100% Digital | Ref. No. | Ref. Name | Ref. Description | Ref. Status | Ref. Phase End | Ref. Status | Ref. Phase End | Ref. Status | Ref. Phase End | Ref. Status | | | |
| | | | | | | | | Ref. No. | Ref. Name | Ref. Description | Ref. Status | Ref. Phase End | Ref. Status | Ref. Phase End | Ref. Status | Ref. Phase End | Ref. Status | | | |
| MIS | SPR-0104 | Natural PLSA - 100% Digital Challenge: not more than 100% digital | Natural PLSA | TLO/OT | MIS/CI/CI | YES | Natural PLSA - 100% Digital | Ref. No. | Ref. Name | Ref. Description | Ref. Status | Ref. Phase End | Ref. Status | Ref. Phase End | Ref. Status | Ref. Phase End | Ref. Status | | | |
| | | | | | | | | Ref. No. | Ref. Name | Ref. Description | Ref. Status | Ref. Phase End | Ref. Status | Ref. Phase End | Ref. Status | Ref. Phase End | Ref. Status | | | |
| MIS | SPR-0105 | Natural PLSA - 100% Digital Challenge: not more than 100% digital | Natural PLSA | TLO/OT | MIS/CI/CI | YES | Natural PLSA - 100% Digital | Ref. No. | Ref. Name | Ref. Description | Ref. Status | Ref. Phase End | Ref. Status | Ref. Phase End | Ref. Status | Ref. Phase End | Ref. Status | | | |
| | | | | | | | | Ref. No. | Ref. Name | Ref. Description | Ref. Status | Ref. Phase End | Ref. Status | Ref. Phase End | Ref. Status | Ref. Phase End | Ref. Status | | | |
| MIS | SPR-0106 | Natural PLSA - 100% Digital Challenge: not more than 100% digital | Natural PLSA | TLO/OT | MIS/CI/CI | YES | Natural PLSA - 100% Digital | Ref. No. | Ref. Name | Ref. Description | Ref. Status | Ref. Phase End | Ref. Status | Ref. Phase End | Ref. Status | Ref. Phase End | Ref. Status | | | |
| | | | | | | | | Ref. No. | Ref. Name | Ref. Description | Ref. Status | Ref. Phase End | Ref. Status | Ref. Phase End | Ref. Status | Ref. Phase End | Ref. Status | | | |
| MIS | SPR-0107 | Natural PLSA - 100% Digital Challenge: not more than 100% digital | Natural PLSA | TLO/OT | MIS/CI/CI | YES | Natural PLSA - 100% Digital | Ref. No. | Ref. Name | Ref. Description | Ref. Status | Ref. Phase End | Ref. Status | Ref. Phase End | Ref. Status | Ref. Phase End | Ref. Status | | | |
| | | | | | | | | Ref. No. | Ref. Name | Ref. Description | Ref. Status | Ref. Phase End | Ref. Status | Ref. Phase End | Ref. Status | Ref. Phase End | Ref. Status | | | |
| MIS | SPR-0108 | Natural PLSA - 100% Digital Challenge: not more than 100% digital | Natural PLSA | TLO/OT | MIS/CI/CI | YES | Natural PLSA - 100% Digital | Ref. No. | Ref. Name | Ref. Description | Ref. Status | Ref. Phase End | Ref. Status | Ref. Phase End | Ref. Status | Ref. Phase End | Ref. Status | | | |



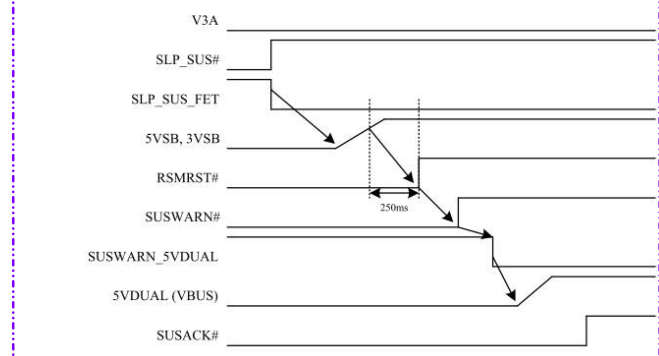




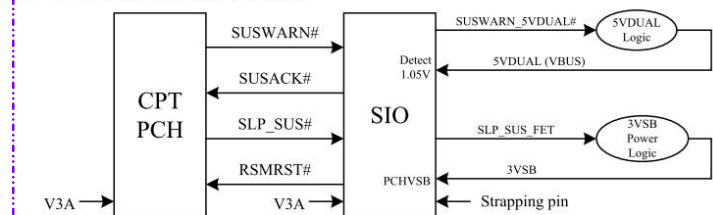




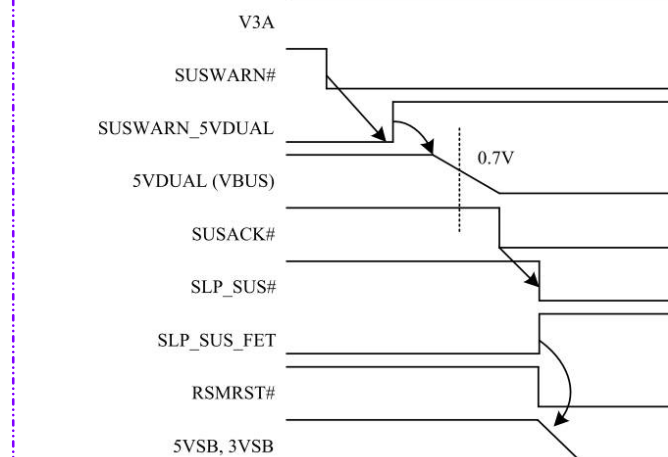
5.9.2 Exit DSW State timing diagram



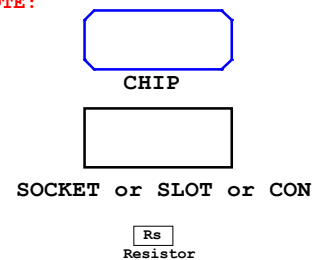
5.9 Fail-safe Intel DSW Function



5.9.1 Enter DSW State timing diagram



NOTE:





Wistron Incorporated

12F, 88, Hsin Tai Wu Rd

Hsichih, Taipei

| Title |
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107_Change History

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